Package Reliability and Integrity Improvements for a Thermally Enhance Non-Conductive Die Attach Adhesive for ASIC Devices on Exposed Pad Packages

Alvin Denoyo, Darwin De Lazo, Ivan Costa, Allen Menor ON Semiconductor Philippines Inc., Carmona, Cavite, 4116 Philippines

Abstract

Polymers being used in a plastic-encapsulated integrated circuit (IC) package exposed to a humid environment absorbed moisture and expand resulting to a so called delamination failure. Weak or imperfect adhesions between the interfaces of the mold compound and adhesive unto the leadframe surface are often the main sources of these failures. In response to automotive requirements and to ensure excellent package reliability and integrity, delamination in all interfaces should then be eliminated. Thus the primary objective of this work is to fulfill the no delamination criteria in all interfaces after moisture soak for an exposed pad package. To satisfy these requirements, activities includes leadframe design improvements, surface enhancement and bill-of-material changes. With the design improvements implemented, still the material compatibility plays an important role in achieving improved package reliability.

Key words: BOM, MSL, Leadframe, Delamination, PPF, NiPdAu, Die attach Adhesive

Introduction

One of the most often failure seen on IC packaging is delamination. In effect, it destroys the package integrity in a form of die crack, wire bond lift or break, thermal and electrical performance degradation. If all interfaces in the package had perfect adhesions and the stresses were small, delamination will unlikely to occur. However, CTE mismatches between material, improper package structures, un-optimized process conditions and extreme environment application temperature and humidity may result to huge interface stresses and internal package delamination. Some researchers used the method of finite element analysis (FEA) to predict the occurrence of delamination under different conditions. Interface shear stress or strain, von Mises stress, J-integrate and energy release rate were usual indicators to assess the delamination. While there were few papers about the effects of processes prior to molding on package delamination [1]. Interfacial delamination is an issue which affects lead frame package reliability. Delamination causing electrical or thermal failure can occur at any interface in a lead frame package involving the silicon die, epoxy molding compound, leadframe and/or die attach ahesive. A survey on delamination of IC packages in electronic products was performed by Ho [2]. As observed, the interfacial stresses will depend on the package geometry, materials and the temperature loading conditions. Without interfacial strength measurements to correlate to the modeled values, the stress required to drive an interfacial delamination is unknown and failure prediction is not possible. Similarly, experimental interfacial adhesion testing by itself is useful for ranking and comparing materials, but is inadequate to determine how high adhesion must be in a package to avoid delamination [3]. Other factors such as surface contaminants on the leadframe, silicon die, and die paddle can prevent perfect adhesion with the epoxy molding compound and may lead to interfacial delamination. Likewise, the use of incorrect leadframe surface finish and coupled with excessive release agents of the encapsulant may also reduce the adhesion strength between the two (2) adjoining surface or interface. Moreover, mismatches between coefficient of thermal expansion (CTE) of the plastic, metal, silicon die and adhesive materials can also result in delamination.

This paper aims to eliminate interfacial delamination occurring after moisture soak and temperature cycles (TC). Additional leadframe design improvements were introduced to enhance mold to substrate locking mechanism as well as new material types were introduced to verify the effect of the said design improvements as well as different material compatibilities. The chosen test vehicle in the course of the study will be based on the worst package affected with interfacial delamination with the biggest silicon die and leadframe paddle dimension available in the factory.

Review of Related Work

Possible failure mechanisms from plastic encapsulated exposed pad package failure modes due to delamination are shown in Figure 1 thru Scanning Acoustic Topography (SAT) test. Images illustrates areas affected with delamination, where

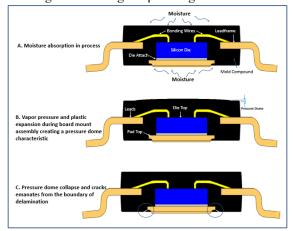
- a) silicon die to mold compound interface;
- b) leadframe die paddle to mold compound interface;
- c) die attach silicon-leadframe interface; and
- d) leadfinger tips to mold compound interface.

Figure 1. SAT Images which illustrates areas affected with delamination



Furthermore, in Figure 2 shows one of the most common end effect failure modes (pop-corning) as a result of delamination, moisture accumulation, and pressure released within a plastic package during the board mounting process [4].

Figure 2. Package Popcorning Mechanism



In Figure 3 shows the typical assembly process flow for a copper based pre-plated frames: 1) sawing wafer into individual dies; 2) die bonding unto leadframe pad area using a die attach adhesive material; 3) die bond curing step; 4) thermosonic bonding of gold wires between bonding (ball) pads on the silicon die unto the leadframe leadfinger tips (stitch); 5) encapsulating the whole structure with molding compound; 6) post mold curing; 7) deflash; 8) marking, and 9) trim, form, and singulation.

Figure 3. Typical Integrated Circuit Assembly
Process Flow



Materials & Methods

On the existing exposed pad SSOP 36-lead package using a non-conductive die attach adhesive, the main defect observed were the delamination seen at the mold compound and die attach adhesive to leadframe paddle interfaces. In order to initially address the issue, leadframe surface roughening treatments as well as design enhancements were introduced to enhance mold locking mechanisms. A copper based with nickel-palladium-gold frame with a paddle size of 4.2x5.8 mm was chosen to carry over lower pad sizes, lead counts, and body sizes while the silicon die size used is 3.1x3.3 mm. Table 1 shows the material properties for all adhesives that will be used in this evaluation. Existing assembly process flow as shown in Figure 3 was utilized in the course of the study. The assembled units were subjected to different moisture soak or moisture sensitivity levels/conditions shown in Table 2 under IPC and JEDEC requirements. A Scanning Acoustic Topography (SAT) images were likewise used to check for delamination in all interfaces.

Table 1. Die Attach Material Technical Data Sheet Comparison

		STANDARD Technical Data Comparison							
	DATA	UNIT	Control	Sample A	Sample B	Sample C			
DATA CATEGORY	APPLICATION		NON- CONDUCTIVE	NON- CONDUCTIVE	NON- CONDUCTIVE	NON- CONDUCTIVE			
	Base Resin	-	EPOXY	BMI Hybrid	BMI Hybrid	BMI Hybrid			
	Appearance	-	White	White	White	White			
	Filler Type		Al ₂ O ₃						
COMPOSITION	Filler Size (max)	um	50	5	10	10			
	Na+ (ppm)	ppm	10	<20	<20	<20			
	Cl- (ppm)	ppm	30	<20	<20	<20			
	K+ (ppm)	ppm	-	<20	<20	<20			
	Recommended LF Plating	-	Ag plated Cu	Cu, Ag, PPF	Cu, Ag, PPF	Cu, Ag, PPF			
PROPERTIES	Viscosity	5rpm, PaS	15	22	16	16			
(i.e. prior PMC)	Thixotropic Index		3	5.1	3.6	6			
(i.e. prior PMC)	Worklife	hours	24	24	24	24			
	Shelf Storage Temperature	•C	-15	-40	-40	-40			
	Elastic Modulus @ RT	MPa	16000	4067	7036	8058			
PERFORMANCE (i.e. after PMC)	Elastic Modulus @ 260 °C	MPa	80	555	1177	839			
(i.e. arter PMC)	Thermal Conductivity (W/m*K)	W/mK	2.0	1.4	3.0	2.8			

Table 2. IPC/JEDEC J-STD-20 MSL Classifications

		Soak Re	Floor Life					
	Star	ndard	Accel	erated	Floor Life			
Level	Time (hrs) °C/%RH		Time (hrs)	°C/%RH	Time	°C/%RH		
1	168 +5/-0 85/85		n/a n/a		unlimited	<=30/85%		
2	168 +5/-0 85/60		n/a n/a		1 year	<=30/60%		
3	192 +5/-0 30/60		40+1/-0 60/60		168 hours	<=30/60%		
4	96 +2/-0 30/60		20+0.5/-0 60/60		72 hours	<=30/60%		
5	72 +2/-0 30/60		15+0.5/-0 60/60		48 hours	<=30/60%		

Results & Discussion

Subjected initially to a 30°C and 60% RH (relative humidity) for 192 hours (MSL 3 soaking condition) and 500TC (-65°C/+150°C) conditions were made to verify the effectiveness the improvements while considering the effect of the adhesive bond line thicknesses as well.

Thru Scanning Acoustic Topography (SAT) results in Table 3 shows that the leadframe design improvements are effective regardless of bond line thicknesses using the existing material. To speed up the experimentation, the next round of evaluation will cover the existing non-conductive die attach material and three (3) new candidates with different material properties together with the improved

leadframe with design and surface enhancements to improve mold-leadframe locking features. Based on materials thermal conductivity and compatibility, together with the new leadframe material, the delamination performance after 85°C and 85% RH for 168 hours (MSL 1) and 85°C and 60% RH for 168 hours (MSL 2) soaking conditions plus 500 and 1000 temperature cycles were checked. SAT results in Table 4 validates that with the existing material, the improvements were proven not effective especially with higher moisture soak requirements which is in contrary with the new adhesives or materials considered. Representative SAT photos of the units that passed and failed the delamination criteria are shown in Figure 5. It confirms that the interface between mold and lead frame is one of the regions that are most susceptible to delamination due to build-up of high stresses and pressure (i.e. due to CTE mismatch and moisture release, respectively). Hence, it is also most susceptible to crack formation during reflow soldering [3].

Table 3. Delamination Results after MSL 3 (30°C/60% RH for 192 hours) + 500TC

	SAT RESULTS (rej/ss)											
	Criteria 1 (Zero delamination over the <u>purface of the die</u> in a clearly defined region)			Criteria 2 (No surface-breaking feature delaminated along its entire length (lead fingers, tie bars, heat spreader, heat slug).			Criteria 3 (Wire bond post can have no delamination adjacent to the bond.)			Criteria 4 (There must be <50% delamination under the surface of the die in the die attach material, rrespective of the type of die attach material/method used.)		
	PREMSL POST POST TO MSL 500			PRE MSL	PREMSL POST POSTTC MSL 500		PRE MSL POST MSL		POST TC 500			POST TO 500
CONTROL	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	18/25	18/25
1-mil BLT	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25
1.5- mil BLT	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25

To further choose the best material for this specific package type, thermal impedance (the sum of its thermal resistance and all contact resistances), Zth values of the new materials were taken as shown in Table 5. With the results, SSOP36-lead Exposed Pad packages using a non-conductive adhesive with high thermal conductivity can now achieve MSL 1 without any form of delamination in all interfaces and even up to 1000TC.

Table 4. MSL 1 & 2 + 1000TC SAT Results

		SAT RESULTS (rej/ss)															
	Lot ID	Criteria 1 (Zero delamination over the <u>surface</u> of the die in a clearly define region)			Criteria 2 (No surface-breaking feature delaminated along its entire length (lead fingers, tie bars, heat spreader, heat slug)			Criteria 3 (Wire bond post can have no delamination adjacent to the bond)			Criteria 4 (There must be <50% delamination under the surface of the die in the die attach material, irrespective of the type of die attach material/method used)						
		PRE MSL	POST MSL	TC 500	TC 1000	PRE MSL	POST MSL	TC 500	TC 1000	PRE MSL	POST MSL	TC 500	TC 1000	PRE MSL	POST MSL	TC 500	TC 1000
	Sample A	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20
	Sample B	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20
MSL 1—	Sample C	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20
Į	Control	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	11/20	20/20	20/20
ſ	Sample A	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20
MSL 2→	Sample B	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20
	Sample C	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20
	Control	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	12/20	12/20	12/20

Figure 5. Representative SAT Photo after 1000TC

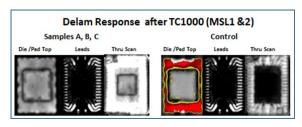


Table 5. Zth Measurement Results

Unit# (Column)	Control	Sample A	Sample B	Sample C
1	15.03	13.23	13.14	12.82
2	15.14	13.14	13.03	12.92
3	15.30	13.36	13.24	12.93
AVG	15.16	13.24	13.14	12.89

Conclusion

Interfacial delamination is one of the most challenging defects encountered IC packaging that often results to other package failures. However, such defect can be eliminated with the right assembly process conditions and with the correct bill of material combination. Material compatibility then plays an important role in achieving improved package reliability. With the above results, SSOP36lead eposed pad packages using a non-conductive adhesive with high thermal conductivity can now achieve MSL 1 without any form of delamination in all interfaces and even up to 1000TC. With Sample C, having the lowest thermal impedance value (with higher thermal conductivity value than the existing material) was chosen to be the best material in the activity.

Recommendations

It is then recommended to perform another confirmation or large scale validation runs prior qualification builds to verify the effect of material lot to lot delivery, variability and process consistency. Furthermore, another set of evaluations will be conducted for conductive adhesives on exposed pad packages.

Acknowledgement

We would like to acknowledge the whole New Product Development team in providing the technical support and to the Reliability Group for the package reliability and test conducted. Likewise, to the staff who provided their skills for the tests and measurements and lastly to ON Semiconductor Management in supporting this activity.

References

[1] Fei Zong, Zhijie Wang, Yanbo Xu, Jiyong Niu, and Yi Che, "Effects of Alternating Thermal Stress on Delamination between Die Attach and

- Leadframe in SOIC Package, Electronics Packaging Technology Conference (EPTC 2013), 2013 IEEE 15th, 2013, pp. 685-690.
- [2] Katherine Ho, Annette Teng, "Survey on delamination of IC packages in electronic products," Electronic Materials and Packaging, 2000 (EMAP 2000) International Symposium, 2000, pp. 269-273.
- [3] Venkat Srinivasan, Mikel Miller, Siva Gurrum, Jie-Hua Zhao, Darvin Edwards, and Masood Murtuza, "Delamination Prediction in Lead Frame Packages Using Adhesion Measurements and Interfacial Fracture Modeling", 2011 Electronic Components and Technology Conference, 2011, pp. 1269-1275.
- [4] "Analysis of Plastic Parts Package Delamination" NASA Electronic Parts Program, November 2005.
- [5] Commercial Off-the-Shelf Parts Evaluation "Delamination Prediction in Lead Frame Packages Using Adhesion Measurements and Interfacial Fracture Modeling", 2011 Electronic Components and Technology Conference, 2011, pp. 1269-1275.
- [6] Mold Compound Suppliers Materials Technical Data Sheets.
- [7] Electronics Industries Association, IPC/EIA/JESD22-A112 Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices.
- [8] Electronics Industries Association, JESD22-A113 Preconditioning of Plastic Surface Mount Devices Prior to Reliability Testing.
- [9] Andrew A. O. Tay band K. Y. Goh, "A Study of Delamination Growth in the Die-Attach Layer of Plastic IC Packages Under Hygrothermal Loading During Solder Reflow", IEEE Transactions on Device and Materials Reliability, Vol. 3, No. 4, December 2003, pp. 144-151.
- [10] A.A.O. Tay, T.Y. Lin, "Effects of Moisture and Delamination on Cracking of Plastic IC Packages During Solder Reflow", Electronic Components and Technology Conference, 1996, pp. 777-782.
- [11] U. Mokhtar, R. Rasid, S. Ahmad, A.E. Said, F.L.A. Latip and C.C. Ng, "Effect of Mold Compound and Die Attach Adhesive Material on QFN Package Delamination and Warpage Issues", Solid State and Technology, Vol. 16, No 2 (2008) 83-91 ISSN 0128-7389
- [12] Edward R. Prack and Xuejun Fan, Intel Corporation, Chandler, "Root Cause Mechanism for Delamination/Cracking in Stacked Die Chip Scale Packages", Intel Corporation, Chandler, Arizona, United States
- [13] I, Fukuzawa, S. Ishiguro, S. Nanbu, "Moisture resistance degradation of plastic LSIs by reflow soldering", Proc. IRPS, 1985, pp. 192-197.