HIGHLY IONIZED SPUTTERING FOR TSV-LINING

Mohamed Elghazzali and Jürgen Weichart
OC Oerlikon Balzers Ltd.
Iramali 18, FL-9496 Balzers, Liechtenstein
Phone: +423 388 5848, Fax: +423 388 6254, mohamed.elghazzali@oerlikon.com
Phone: +423 388 4271, Fax: +423 388 6254, juergen.weichart@oerlikon.com

Abstract

The barrier and seed layers for electroplating of copper play a critical role in the realization of through silicon vias (TSV) in 3D IC packaging. Physical vapour deposition (PVD) is still the preferred method for depositing these films, but must meet the technical challenges presented by the need to line high aspect ratio vias of 10:1 or more that often have rough sidewalls, and the market demand of low cost. A bilayer of TaNx/ α-Ta is the preferred diffusion barrier for copper metallization in CMOS multilevel damascene structures, providing a good adhesion and wetting layer for the PVD copper seed layer. A new method called Highly Ionized Sputtering (HIS) has been developed using power pulses of 50 to 200µsec length with a low duty cycle but very high peak current of several hundred amps. The high pulse current generates a very high ionization fraction of the sputtered material giving – with an appropriate bias voltage applied to the wafer – a high directionality of metal ions and providing very dense films as needed for the diffusion barrier. HIS uses regular sputtering equipment, planar targets and works at low target-to-substrate distances thus providing excellent transfer factors of the ionized PVD material, resulting in high target utilization and a low cost of ownership. HIS hardware and processes with competitive deposition rates, good uniformities and low stress have been developed on the Oerlikon 200mm and 300mm PVD cluster tools for TaN_x, Ta, Ti and Cu. The applicability has been verified experimentally in TSVs with different sidewall qualities and supported by simulations.

Key words: 3D packaging, IPVD, TSV, copper seed, diffusion barrier, alpha tantalum

Introduction

The development of 3D IC packaging allows an increase in integration density and higher functionality in smaller and smaller packages. Here, the electrical connections between the stacked chips are no longer wire bonded: they are realized by vertical through-silicon vias (TSV) [1, 2] connecting the front and the back side of a substrate, usually through thinned silicon wafers. Several approaches of via application have been described, from “via first” to “via last” or the use of interposer wafers [3]. The future trend towards features with very high aspect ratios requires improvements to the deposition technologies used today. The basic steps to produce a filled via are: (i) insulating the via from the surrounding silicon substrate; (ii) deposition of the barrier and seed layers; and (iii) electroplating to fill the feature (typically with Cu). For the deposition of the barrier and seed layers, physical vapour deposition (PVD) is preferred to chemical vapour deposition (CVD) and wet chemical techniques because it combines superior film quality at low deposition temperatures with better adhesion to the underlying substrate, and provides easy and safe processing (when compared to metal CVD). However for deposition in features with high aspect ratios, directional sputtering is needed, either by collimation or by ionized PVD (IPVD) [4, 5]. There are several existing solutions, most of which suffer from complex hardware geometry of the targets and shields and/ or the risk of particle generation (especially from collimators). This has led to the development of a new IPVD technology as described in the following section.

The principle of highly ionized sputtering (HIS)

HIS is a pulsed DC process that uses power pulses of 50 to 200µsec length with a low duty cycle but with a very high peak current of several hundred amps; this produces peak powers on the target up to several MW [6, 7]. Using this technique, very high plasma densities can be achieved.

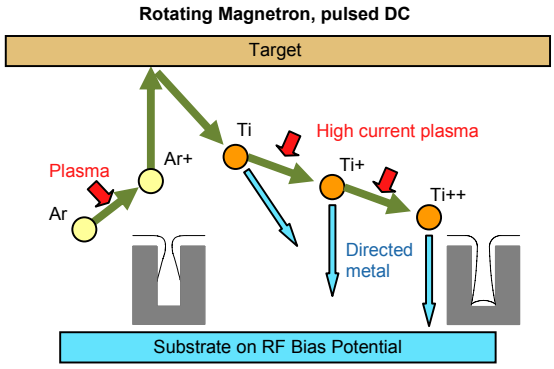

Fig. 1: HIS schematic principle

A physical model describing the HIS principle is depicted in Fig. 2. From a rotating magnetron source, metal atoms – indicated as Ti – are sputtered by argon ions. These metal atoms typically have a relatively wide angular distribution

which results in poor deposition profiles in deep features, as indicated in the left insert in Fig. 1. Due to the very high plasma currents in HIS, the neutral metal atoms are ionized to Ti^+ ions; even multiple ionizations into Ti^{2+} are possible. By applying an RF bias on the substrate, a potential difference between the plasma and wafer surface develops; ionized metal is accelerated across the sheath in a very narrow angular distribution. This makes it possible to deposit continuous layers in deep features as indicated in the right insert of Fig. 1. In addition to the high directionality of the depositing material, very dense metal films can be produced by HIS as are needed for diffusion barriers.

The ionization of the sputtered material depends on the pulse energy applied to the target: this is determined by the pulse voltage, the pulse length and the pulse current. Ionization fractions of ≥90% have been reported in the literature [8]. Furthermore, by adjusting the pulse frequency, the average power and therefore the deposition rate can be controlled. However, the maximum average power is typically limited by the ability to effectively cool the source.

HIS process development

It is usually straightforward to apply HIS to any existing PVD source such as the regular Oerlikon magnetron source, the ARQ151. This source uses a 300mm planar target with a very simple geometry, a rotating magnetron for full face erosion and has a high target utilization in stationary sputtering. The degree of ionization degree generated by this source when equipped with a titanium target has been quantified by using atomic absorption spectroscopy (AAS) installed at a distance of 130mm from the source [9]. These measurements have shown that the degree of ionization calculated by the relation:

$$\frac{n(Ti^+)}{n(Ti^+)+n(Ti^0)}$$

could be increased from 26% to 46% when the peak pulse discharge current was adjusted from 180A to 1000A. Additionally, at high currents, the ionization of metal vapour was so intense that the density of the atomic Ti^0 started to decrease since neutrals were consumed and converted to metal ions.

All of the following experiments were performed either on the Oerlikon Clusterline® 200-II with the ARQ151 source (for 200mm wafers) or on the Clusterline® 300-II with ARQ310 source (for 300mm wafers). The latter uses a planar target of 400mm diameter and adjustable magnets that control deposition uniformity over target life as described elsewhere [10]. The Clusterline system consists of a central transfer chamber to which as many as six process modules can be attached, as shown in Fig. 2.

The system used for this work was equipped with two turbomolecular-pumped load lock stations for 25-wafer cassettes. The transfer module included a two-arm robot, which transported the substrates from the load lock to the process modules and an integrated alignment system (mechanical and optical) for accurate orientation of the wafer. In addition, the system contained integrated degas and cooling modules.

During processing, the wafer was first transferred from the load lock to the aligner and degas station, followed by sputter etch cleaning in an inductively coupled etch station. Two PVD chambers on each system were dedicated for HIS depositions, one for the diffusion barriers and adhesion layers of titanium or tantalum and one for the copper seed layer. HIS was incorporated onto the system with only a few minor changes (essentially just a different magnet system and new electrical connections). The PVD source, shields and chucks (the latter equipped with mechanical clamps and active back-gas cooling) remained unchanged. RF bias was applied to the chuck with matching appropriate for HIS.

HIS hardware and processes with competitive deposition rates, good uniformities and low stress have been developed on both ARQ151 and ARQ 310 for TaN, Ta, Ti and Cu.

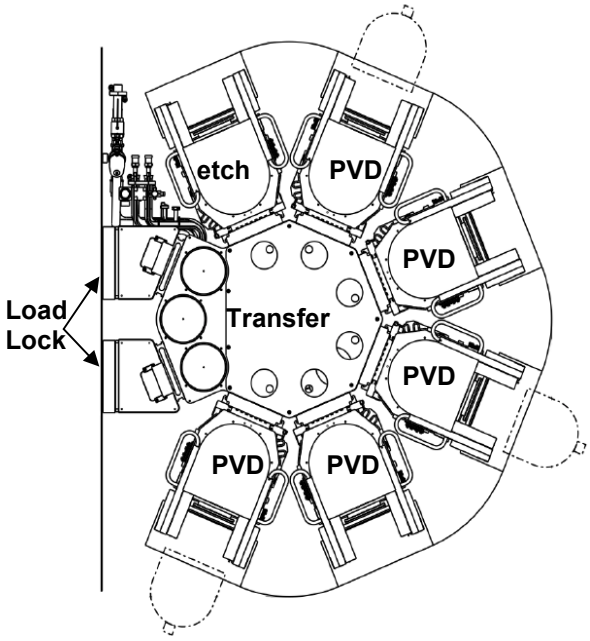

Fig. 2: Clusterline® 200-II schematic principle

Film characterization

Various analytical methods were used to characterize the film properties and optimize the process parameters. The sheet resistance of a layer depends on the microstructure of the deposited material and is therefore an important parameter when characterizing a film. An automatic four-point probe Omnimap RS-100 from KLA Tencor was used for these measurements.

The film thickness was measured by a Veeco step profiler (300mm) and the specific electrical resistivity was calculated from the film thickness and sheet resistance.

The stress of a deposited layer is composed of the thermal stress and the intrinsic stress induced by the microstructure of the layer. The film stress was measured with a KLA Tencor FLX-2320 on 200mm wafers and with a Veeco profiler on 300mm wafers.

The film structure and orientation was analyzed by X-ray diffraction, specifically for Ta on an X-Pert PRO MRD XL from PANalytical.

Step coverage in the vias was analyzed using Focussed Ion Beam Secondary Electron Microscopy (FIB-SEM) supported by EDX (Zeiss 1540 XBeam).

Substrate temperature

Temperature control during deposition has a vital impact on the deposition results. Most important, in many IC packaging applications the maximum allowable temperature is <150°C. In addition, thermal stress can cause wafer bow or delamination of the film. When Cu is deposited at too high a temperature, agglomeration of the layer can occur (as illustrated in Fig. 3, where the substrate was decoupled from the cooled chuck by turning off the back-gas). Subsequent electroplating of a feature with an agglomerated Cu seed layer results in discontinuities and voids in the via.

A typical Cu film thickness in this work was 1200nm, requiring thermal coupling of the substrate with Ar back-gas to an actively cooled chuck maintained at -20°C. After continuously processing 25 wafers sequentially through the tool with the following process flow – 30nm etch / 600nm Ti / 1200nm Cu –at a throughput of 15 wafers per hour, the substrate temperature for a standard Si wafer stayed below 140°C.

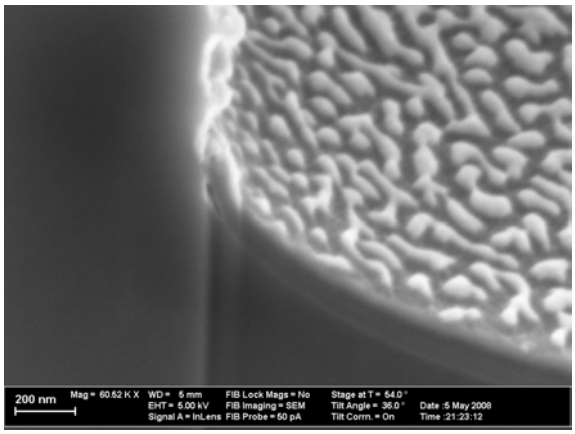

Fig. 3: Cu agglomeration in the via at elevated temperature

Experimental results

The film properties achieved on 200mm and 300mm wafers are summarized in Table 1. Measured deposition rates, specific resistivity, uniformity and stress meet the demands of IC packaging. In the case of a Ti/Cu process, the lower deposition rate of Ti does not negatively impact the overall process throughput since the latter is primarily governed by the higher deposition rate of the thicker Cu film. Also, the compressive stress of Ti and Ta is compensated by the tensile stress of the thicker Cu layer.

Table 1: Film properties of Ti, Ta and Cu produced by highly ionized sputtering (HIS) on 200mm and 300mm Clusterline®

	Deposition Rate	Specific Resistivity	Resistance uniformity, on 300mm	Resistance uniformity, on 200mm	Film stress
Material	[nm/s]	[μΩ-cm]	1/2 range/mean	1/2 range/mean	[MPa]
Ti	3.1	70	± 5 %	± 3 %	-560
α-Ta	5.4	26	± 6 %	± 4 %	-750
Cu	5.8	2.7	± 6 %	± 4 %	+160

Tantalum-based films are of particular interest and well-established as diffusion barriers in Cu metallisation due to their chemical and thermal stability and their good adhesion. Tantalum has two crystalline phases: the low resistivity (15-60μΩ-cm) alpha (body centred cubic) phase and a higher resistivity (150-210μΩ-cm) beta (tetragonal) phase. Due to the lower resistivity of the alpha phase, it is preferred to the beta phase as a barrier in electronic applications [11,12,13]. As discussed in the literature, there are three main methods to induce tantalum to grow in its alpha phase: 1) controlling the substrate temperature during deposition; 2) adjusting the amount of gaseous contamination in the vacuum system; and 3) depositing a seed layer that promotes the formation of α-Ta as it is

deposited [14, 15, 16]. Fig. 4 shows a schematic of a film stack where a thin TaN_x layer on an SiO_2 insulation layer is used as a seed layer for α-Ta. TaN_x can be deposited by adding a small amount of nitrogen to the HIS process and provides a lattice that promotes α-Ta formation during subsequent deposition.

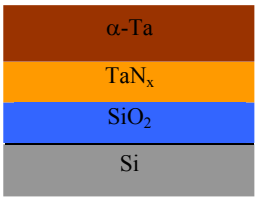

Fig. 4: Film stack used for α-Ta deposition by HIS

Fig. 5 shows the X-ray diffraction pattern (θ-2θ plot) of a 600nm Ta film deposited on a 10nm TaN_x seed layer clearly showing the crystalline structure of α-Ta. Further investigations have shown that a seed layer of even less than 0.5nm of HIS TaN_x provides high quality α-Ta. This fact is important since inside the via, where less material will be deposited, α-Ta growth can still be expected. The specific resistivity of α-Ta deposited by the HIS process is in the range of 18 to 28μΩ-cm, with an average of 26 μΩ-cm, as summarized in Table 1.

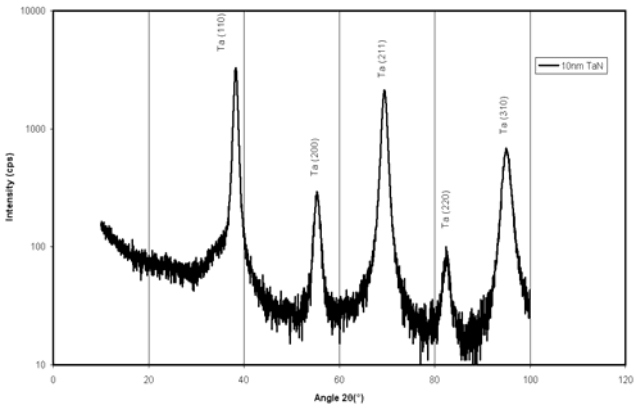

Fig. 5: 600nm Ta deposited with 10nm TaN seed layer (XRD using grazing incidence diffraction)

Experimental results in 10:1 vias

Despite its advantages, HIS is not without several intrinsic limitations that results from the directional nature of its deposition. To illustrate these limitations, two examples of FIB-SEM sectional micrographs from deep silicon etched (DSE) via structures are shown in Fig. 6. On the left of the figure, a via with a highly scalloped sidewall of 1μm depth is shown. It is expected that the negative slopes will not be continuously coated by directional sputtering resulting in voids in either the PVD coating, the electro-deposition or both. The right part of the figure illustrates how a very narrow via, for example, with a diameter of 2μm, can have its opening closed when layers of similar thickness to those used in this work are deposited, thereby preventing further deposition in the feature.

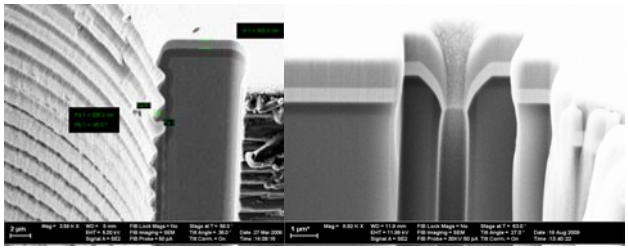

Fig. 6: FIB-SEM micrographs showing principal directional PVD and HIS limitations

However, with medium-sized vias of approximately. 10μm diameter that have smooth sidewalls, good results can be achieved. This was demonstrated on 100μm deep vias with an opening of 8μm and a narrow pitch (Fig. 7). The right upper part of this figure shows how the SiO_2 layer smoothes the scallops while the lower section of this figure shows smooth, flawless TaN_x/α-Ta HIS layers in the bottom of a via with an aspect ratios of 12:1.

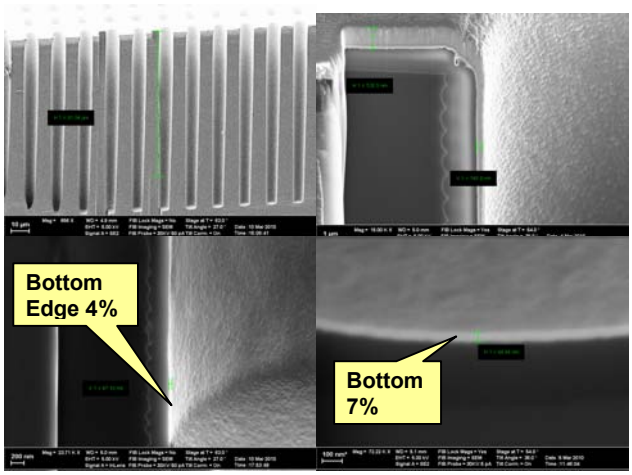

Fig .7: FIB-SEM analysis of Ta(N)/α-Ta layers in ~12:1 vias

The deposition profile along the via side walls has been measured for two samples with these TaN_x/α-Ta HIS layers and the film thicknesses as a percentage of the coating on the field of the substrate is plotted in Fig. 8. In the same figure, a line of the approximated deposition profile is given. This approximated deposition profile can be used to estimate the overall material distribution in the via.

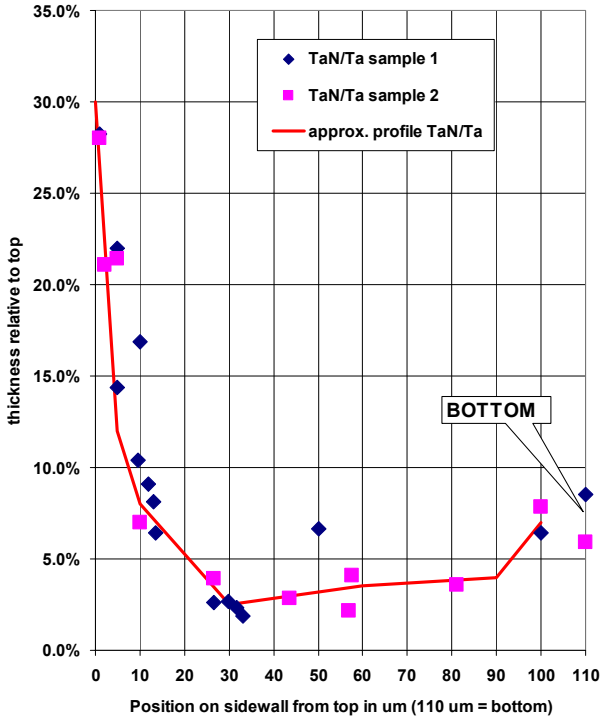

Fig. 8: Deposition coverage profile along the via walls for tantalum in the 12:1 via

For these calculations, the inner surface of the via was divided into surface shell segments as depicted in Fig. 9. For each segment, the volume of the deposited film therein was calculated by multiplying the via circumference, the length of the segment and the film thickness in that segment as given by the approximated deposition profile. The individual volumes of the material on the via walls was summed and added to the volume of the small cylinder of material deposited on the via bottom. This integrated volume was then divided by the volume of the film that deposited on an area of the field corresponding to the area of the via opening (shown as a red disc in Fig. 9). This model calculates the factor by which the volume of material deposited over the internal surfaces of the via exceeds the volume of material that would have deposited on an area of the field immediately above the via opening. In the case of Ta, this factor was 2.66, which suggests that tantalum atoms and/or ions have a high sticking probability in the via. The corresponding factors for Ti and Cu were ~1.8 and ~1.3, respectively, as shown in Figs. 10 and 11.

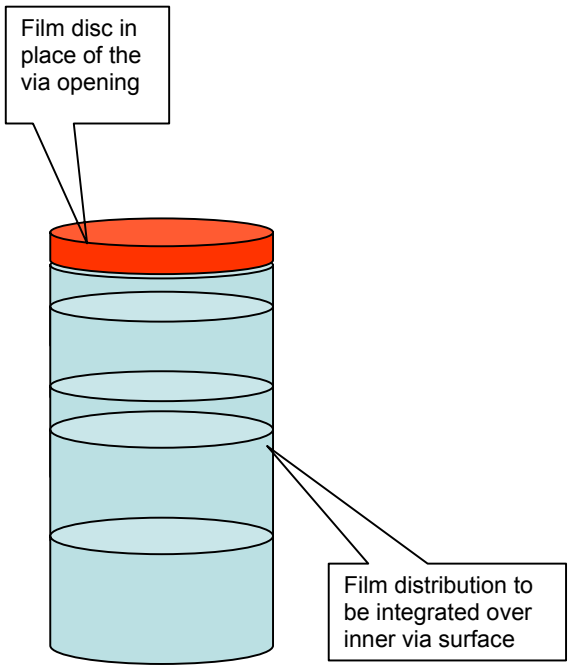

Fig. 9: Model of the film distribution in the 12:1 via

Table 2: The model of approximated distribution in the via

via diam	8	um
via depth	100	um
film	1	um

via entrance layer	50.27	um3		

x	tube heigth		mean%	volume	
2.5	5		21.0%	26.39	um3
7.5	5		10.0%	12.57	um3
20	20		5.3%	26.39	um3
45	30		3.0%	22.62	um3
75	30		3.8%	28.27	um3
95	10		5.5%	13.82	um3
bottom			7.0%	3.52	um3
		sum		133.58	um3
		factor		266%	

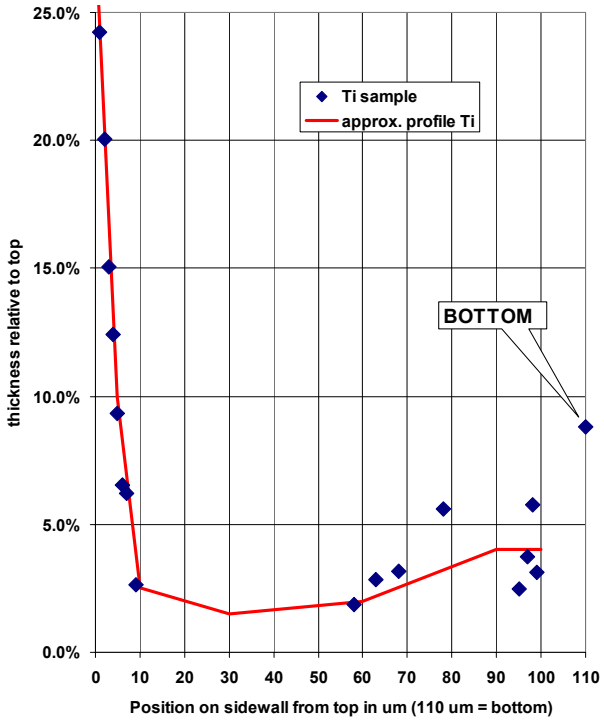

Fig. 10 Deposition coverage profile along the via walls for Titanium in the 12:1 via

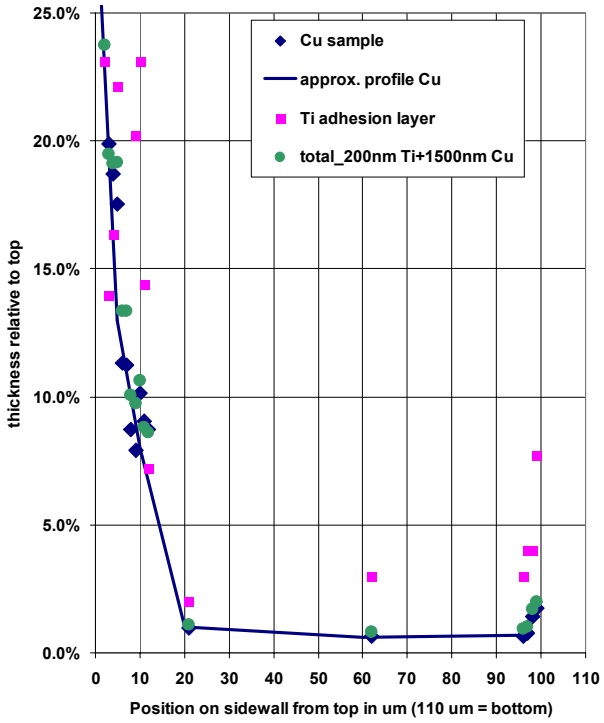

Fig.11 Deposition coverage profile along the via walls for Copper in 12:1 via

Conclusions

A new IPVD technology, called highly ionized sputtering (HIS), has been developed for deposition in features with high aspect ratios for future through-wafer via applications. The material sputtered by HIS shows a high directionality of metal ions that produce very dense films as needed for diffusion barriers, such as α-Ta. HIS technology offers bottom and sidewall coverage results comparable with or even better than other ionized PVD techniques. We demonstrated stable substrate temperature control that met the requirements for IC packaging at a throughput of 15 wafers per hour.

HIS requires only minor modifications to standard PVD components. This makes for a very competitive (even attractive) way to retrofit existing tools, resulting in a low cost of ownership for existing PVD equipment. In particular the plain design of easily exchangeable shields and relatively small target size offer a cost advantage. Compared to other directional PVD techniques, its better bottom and sidewall coverage, denser films, higher target utilization and higher throughput, make it the preferred new tool solution for the IC packaging industry. However, as with all directional deposition techniques, it is important to appreciate the limitations of HIS in order to achieve optimal results in any subsequent electroplating step.

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