3D SiP Assembly and Reliability for Glass Substrate with Through Vias

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Abstract

Applications of Glass substrate for high performance system-in-package (SiP) products have gradually become a promising technology in recent years. Research and development activities are reported in many journal papers and conferences [1, 2]. Consortiums and Alliances are also formed to gather worldwide efforts for developing glass technology. In the past, we have published our development efforts on the process of producing glass substrate with through via and build-up redistribution circuit layers (RDLs) [3]. N. Koizumi [4] first reported glass reliability issues in 2013; and the phenomena he called SE-WA-RE has caused a great concern of using glass as a substrate. Model simulations have indicated that the glass crack is related to the stress buildup by the materials and structure. In this study, we selected a dielectric material/structure set that is designed to be less stressful to the glass substrate. A better reliability result can be expected.

In this paper, we will discuss an assembly structure of SiP module using the glass substrate with through-glass via (TGV) where the diameter of TGV is 100μm with thickness at 200μm. The copper plating technique to form the through via conductor is called direct-metal-on-glass (DMoG) which deposits titanium and copper directly on glass both in the wall of through vias and on glass surfaces of both sides. The first RDL is formed on both surfaces of glass substrate by semi-additive plating (SAP); then followed by build-up RDLs on top of the DMoG RDLs on both sides of the substrate also by SAP with interconnect vias to form connections between DMoG RDLs and build-up RDLs. Finally, solder mask is applied on both sides of the glass substrate leaving pad openings (SRO) for surface finish, die mounting and printed-circuit board connection purposes. At die mounting side, the SRO is 60μm in diameter with minimum pitch at 150μm. The TGV conductors connect the DMoG RDLs on both sides of the substrate. A mechanical test die with 18μm bump diameter is mounted on the build-up RDL at the substrate top side with daisy-chain design both in the test die and TGV substrate RDLs. Thus, the daisy-chain connection can go from the build-up RDL of the substrate back side to the test die on the top side of the substrate. 200 thermal-cycling test (TCT) has been performed and the daisy-chain resistances are measured before and after the 200 TCTs. It is found that 96% of daisy-chains have less than 10% of resistance change after 200 TCTs.

Key words

Glass, Through via, Substrate, Interposer, SiP

I. Introduction

Glass has a unique electrical property which has advantages over silicon and polymer substrates in some electronics applications. IDM/ODM companies are pushing hard to the industry for the development of glass substrates/interposers to provide the need for high performance system-in-package (SiP) products. One feature is specially needed to meet the high performance requirement and that is the through-glass via (TGV). Up until now, the making of TGVs is still a challenging task, especially the via size, the through-put for via quality and cost purposes. Our team has joined a worldwide effort for developing glass technology and our focus is more on the TGV substrate process, assembly and reliability. In this paper we would like to discuss our recent development result of a SiP module using the glass substrate with TGVs as conductors connecting the circuit traces on both sides of the glass substrate. There are several different ways of making the TGV conductors. One method is called via-in-via (ViV) which laminates dielectric layers first on both sides of glass surfaces and later make through holes in the via of the glass substrate. The copper is later deposited

both on the side wall of the dielectric through hole and on the top surface of the dielectric material. The ViV TGV is first reported by [5]. The second method is called direct-metal-on-glass (DMoG) which deposits copper directly on glass both in the wall of through via and on glass surfaces. Detailed process will be described in the following sections.

II. Design Rules of TGV

Figure 1 shows the cross-sectional view of our TGV structures for DMoG design nomenclatures. Tables 1 and 2 indicate the detailed specifications of the design rules and the material set.

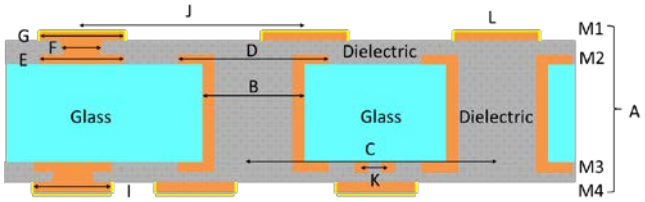

Figure 1 Cross-sectional view of TGV structures

Table 1 Design rules for both the DMoG substrate

Code	Item	Dimension
A	Structure	1/2/1
	Body size (mm)	20 x 20
B	TGV Top/Bottom diameter (µm)	100/90
C	TGV pitch (µm)	150
D	PTH pad diameter (µm)	130
E	Landing pad diameter (µm)	100
F	Via Top/Bottom diameter (µm)	70+/-10 / >50
G	Capture pad diameter (µm)	110
I	SRO diameter (µm)	250
J	Bump pitch (µm)	150
K	Line/Space (µm)	30/30
L	Bump (µm)	60

Table 2 Material set for both the DMoG substrate

Structure	Material type	Spec. (µm)	Tolerance (µm)
Core material	Corning Willow Glass	200	+/-10
Insulator materials	ABF GXT31WR	30	+/-6
BU Cu plating	Cu Thickness	10	+/-2.5
Surface finish	ENEPIG	Ni: 5 Pd: 0.1 Au: 0.1	+/-1 +/-0.03 +/-0.03
Total thickness		330	24

III. Test Chip and Substrate Designs

The SiP module in this study is to emulate an application processor mounted on a glass substrate with TGV. Daisy chain RDL is designed into the TGV substrate and connected with the daisy chain RDL on the test die. Figure 2 illustrates a schematic over view of the test die mounted on the TGV substrate. Figure 3 is an enlarged view of the connection between the test die RDL and the TGV through the substrate RDL.

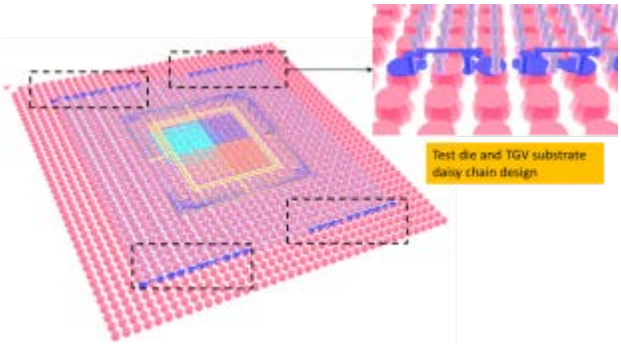

Figure 2 Schematic over view of the test die mounted on the TGV substrate.

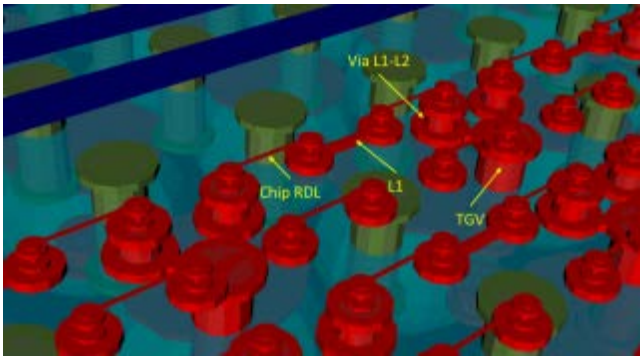

Figure 3 an enlarged view of the connection between the test die RDL and the TGV through the substrate RDL.

The test die is a mechanical silicon chip includes daisy chain RDL and micro bumps. Part of the RDL is designed to be a resistor which can perform as a heater such that the test die becomes a thermal chip when the RDL is powered by electrical current. The die size is 9mm by 9mm populated with 2904 micro bumps and the diameter of the micro bump is 18µm. The minimum line/space of the test die RDL is 6µm/6µm. Figure 4 shows the micro bump and RDL patterns of the test die.

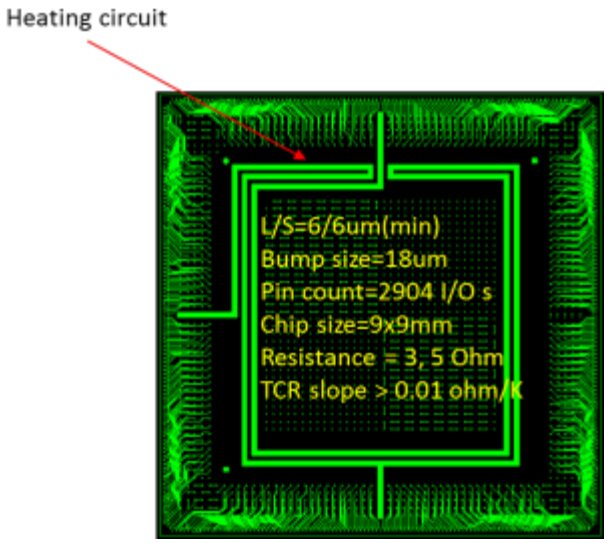

Figure 4 the micro bump and RDL patterns of the mechanical silicon test die.

The unit size of TGV substrate is 20mm by 20mm. Figure 5 shows the design patterns of each layer of TGV substrate from the top side solder resist opening (SRO-TOP) at the upper left to the bottom side solder resist opening (SRO-BOT) at the bottom left.

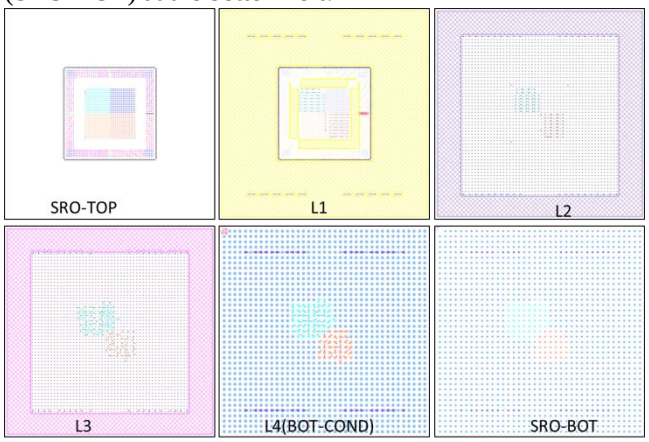

Figure 5 design patterns of each layer of TGV substrate.

Then, the units of TGV substrate are populated on a 150mm by 150mm glass panel. There are total of 28 units can be accommodated in a glass panel. Figure 6 demonstrates the panel design of the TGV substrate units. The RDL build-up after the DMoG RDL on the TGV substrate was attached to an organic core panel with the size of 508mm by 508mm. The RDL patterns on top of the DMoG RDL were defined by laser direct imaging (LDI). With the seed layer forming by chemical deposition and SAP processes, the build-up RDL layers on both sides of glass substrate were successfully formed.

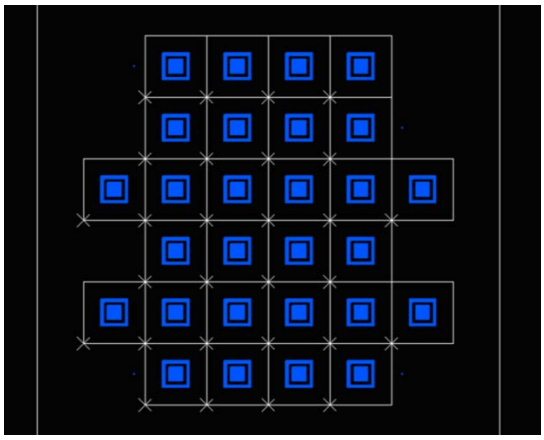

Figure 6 the panel design of the TGV substrate units.

IV. Process of TGV Substrate

In present study, the TGV conductors are fabricated by sputtering titanium and copper (0.05/0.1µm) as a seed layer directly on glass both in the wall of through vias and on glass surfaces. The first RDL is formed on both surfaces of glass substrate by semi-additive plating (SAP) technique. During the first RDL process, the copper thickness of TGV wall is also plated up by SAP. The first RDL is called the DMoG RDL. Then, the DMoG RDL is laminated with dielectric material on both sides of the TGV substrate followed by build-up RDLs on top of the DMoG RDLs on both sides of the substrate also by SAP with interconnect vias to form connections between DMoG RDLs and build-up RDLs. Finally, solder mask is applied on both sides of the glass substrate leaving pad openings (SRO) for surface finish, die mounting and printed-circuit board connection purposes.

Figure 7 shows the cross-sectional view of a SEM picture for the TGV structure as well as the DMoG RDL and the RDL on the dielectric layer connected by an interconnect via. The TGV diameter and the thickness of the glass are also shown in Figure 7.

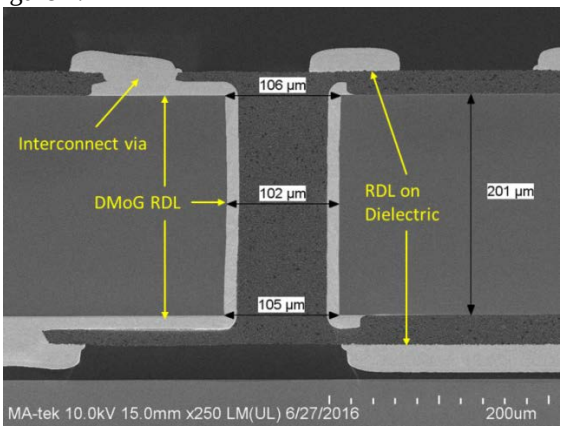

Figure 7 SEM Cross-sectional view of TGV structures.

The copper thickness in the TGV via is measured at 11µm as shown in Figure 8.

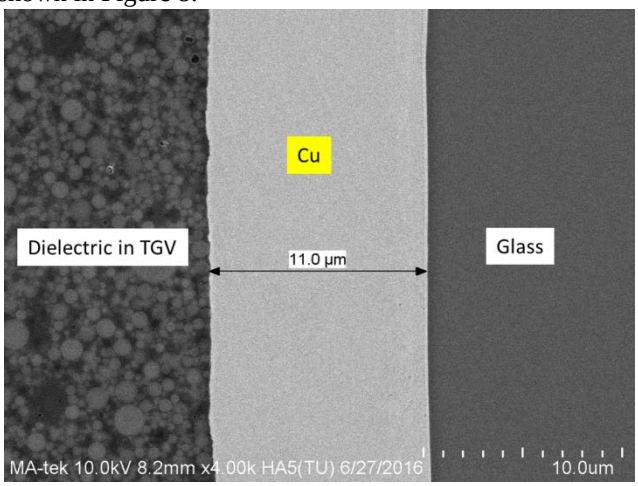

Figure 8 copper thickness in TGV measured from the SEM picture.

V. SiP Assembly

After the DMoG substrate is fabricated as shown in Fig. 6, the substrate units are cut into ribbons (4 and 6 units, respectively) to get ready for assembly with the mechanical test dice to form SiP modules. The test dice are mounted on the ribbon by using a thermal-compression bonder. A non-conductive film (NCF) is placed in between the test die and the substrate to enforce the bonding strength between the test die and the substrate. Figure 9 demonstrates the top view of the first two SiPs after the assembly.

Figure 9 the top view of the first two SiPs after the assembly.

The daisy chain resistance measurement is then conducted immediately from the bottom side of the substrate using 4-wire measurement technique. Figure 10 demonstrates the measurement set-up of daisy chain resistance for SiP.

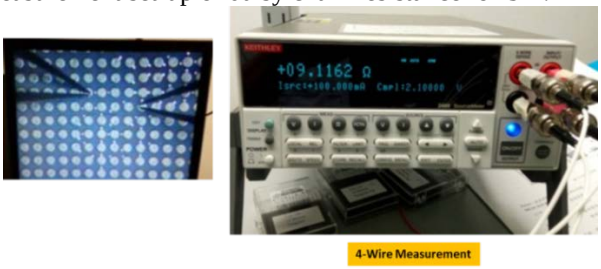

Figure 10 the measurement of daisy chain resistance for SiP.

Figure 11 shows the statistic of daisy chain resistance measurement for one section of the daisy chain groups before the first two SiP modules were sent for TCT reliability test. Some connections between the test die micro bump and substrate contact pad are shown not connected. Therefore, inspections are first conducted with the technique of non-destructive 3D X-ray microscope.

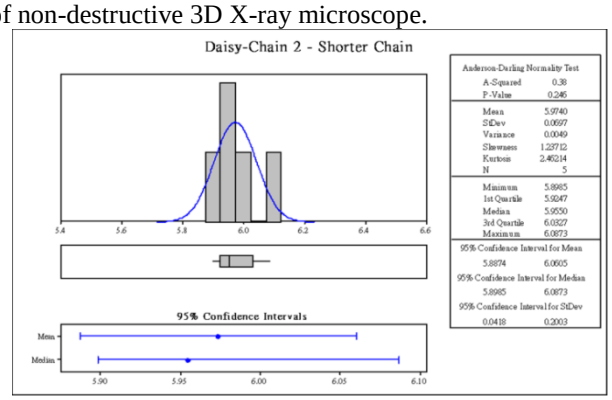

Figure 11 the statistic of daisy chain resistance measurement for one section of the daisy chain groups before TCT reliability test for the first two SiP modules.

Figure 12 shows the over view of the metal circuit for the entire SiP module including micro bumps, contact pads, DMoG RDLs, TGVs, substrate RDLs and solder pads. Figure 13 shows an enlarged view of the TGVs.

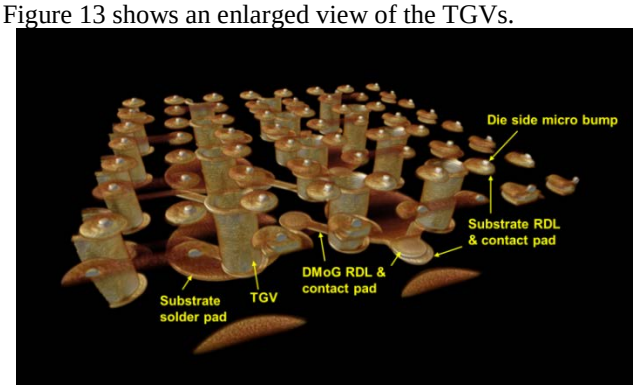

Figure 12 the over view of the metal circuit for the entire SiP module.

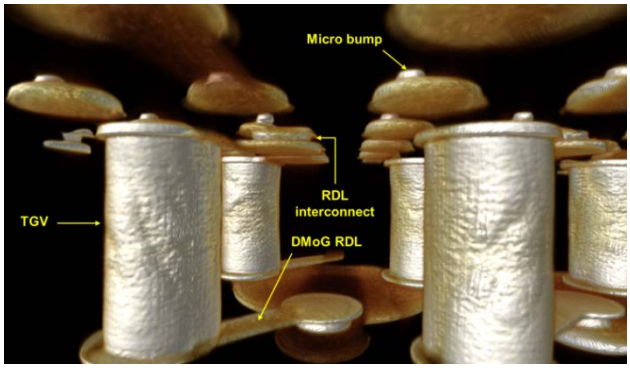

Figure 13 an enlarged view of the TGVs.

In order to locate the failure of daisy chain, a full scan of the cross-sectional view of the entire SiP module is conducted with 3D X-ray microscope. Figure 14 and Figure 15 show a comparison of the normal and abnormal micro bump connections with the substrate RDL contact pads. Based on the comparison of these two figures and indicated by the arrows in Fig. 15, it is highly suspected that the failure of the daisy chain is caused by the uneven surface of nickel plated bonding pad. For further confirmation of this defect, micro-section and SEM inspection will be followed.

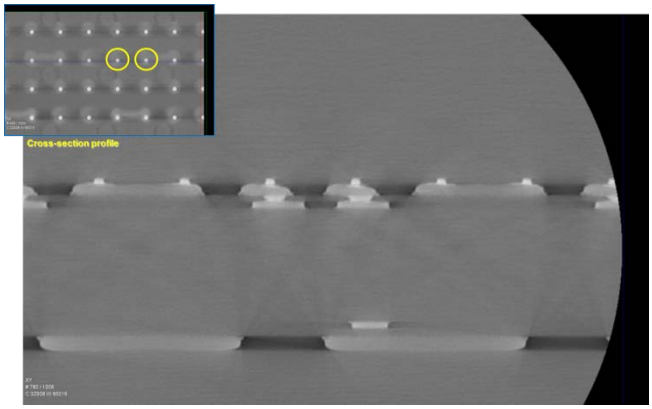

Figure 14 normal bump connections between micro bumps and substrate RDL contact pads.

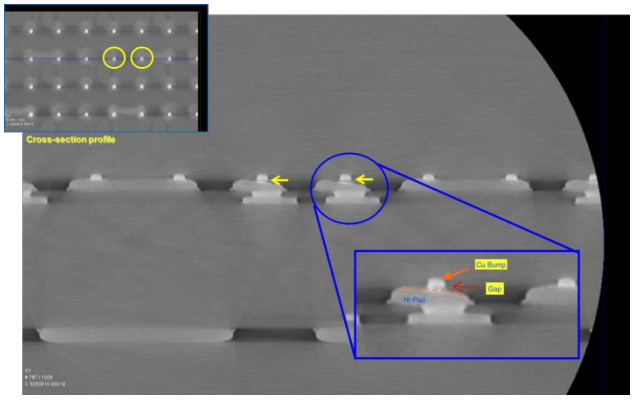

Figure 15 abnormal bump connections between micro bumps and substrate RDL contact pads.

VI. Test Results

Once both samples of the SiP modules have been completed with the chip assembly, daisy chain resistance was measured. Later, the sample #2 is sent to the chamber for the TCT reliability test and the sample #1 is taken to the lab for X-ray and cross-sectional SEM examinations. Table 3 shows the results of the resistance change of all daisy-chains after 200 TCTs. The daisy chains are divided into three groups, i.e. group 1, group 2 and group 3. For group 1, every daisy chain connects 4 micro bumps. For group 2, there are five daisy chains that connect 8 micro bumps, respectively. For group 3, there are three daisy chains that connect 12 micro bumps, respectively. The more micro bumps the daisy chain connects, the longer RDL length of the daisy chain. According to the data shown in Table 3, the linear increase of the resistance is quite consistent with the length increase of daisy chains.

Table 3 the results of the resistance change of all daisy-chains after 200 TCTs.

Daisy chain	Net name	Number of bumps	Before TCT (Ω)	After TCT (Ω)	Resistance change (Ω)	Resistance change (%)
Group_1	G1.1	4	2.9803	3.0835	0.1032	3.46%
	G2.2	4	3.0518	3.2695	0.2177	7.13%
	G1.3	4	2.9901	3.0727	0.0826	2.76%
	G1.4	4	2.9884	3.1543	0.1659	5.55%
	G1.5	4	3.1380	3.3825	0.2445	7.79%
	G1.6	4	2.9731	3.1078	0.1347	4.53%
	G1.7	4	2.9532	3.0180	0.0648	2.19%
	G1.8	4	2.9744	3.1003	0.1259	4.23%
	G1.9	4	3.0653	3.2975	0.2322	7.58%
	G1.10	4	2.9690	3.0512	0.0822	2.77%
	G1.11	4	3.1995	3.5078	0.3083	9.64%
	G1.12	4	3.0623	3.1961	0.1338	4.37%
	G1.13	4	2.9972	3.0808	0.0836	2.79%
	G1.14	4	3.3361	3.5945	0.2584	7.75%
	G1.15	4	2.9969	3.0911	0.0942	3.14%
	G1.16	4	3.1616	3.1878	0.0262	0.83%
	G1.17	4	3.0051	3.1758	0.1707	5.68%
Group_2	G2.1	8	5.959	6.0535	0.0945	1.59%
	G2.2	8	6.0222	6.156	0.1338	2.22%
	G2.3	8	6.0547	6.2102	0.1555	2.57%
	G2.4	8	6.0152	6.1203	0.1051	1.75%
	G2.5	8	6.297	7.9570	1.6600	26.36%
Group_3	G3.1	12	9.0323	9.3226	0.2903	3.21%
	G3.2	12	9.0045	9.3269	0.3224	3.58%
	G3.3	12	8.9802	9.1879	0.2077	2.31%

Table 3 also shows that there are 25 daisy chains under measurements for the resistance change before and after the TCT. Only one daisy chain in group 2 (highlighted in red) is found to result in 26% increase of resistance. The rest of the daisy chains result in less than 10% increase of resistance. Figure 16 demonstrates a chart for the distributions of resistance changes for all daisy-chain groups.

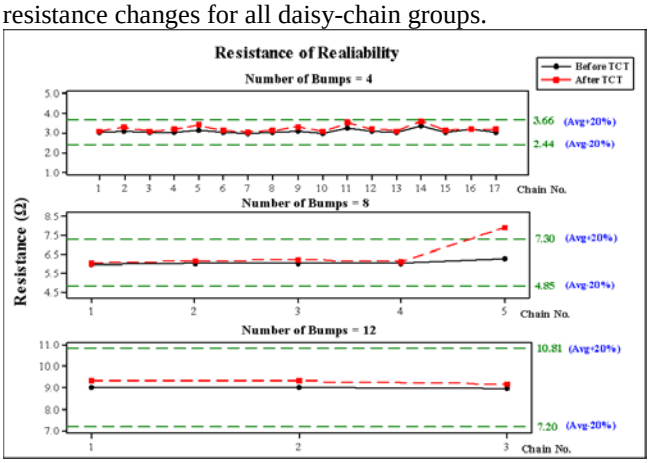

Figure 16 the distributions of resistance changes for all daisy-chain groups.

Figure 17 shows the means variation of the resistance for all groups before and after the 200 TCTs. The mean resistances for all three groups are increased after the 200 TCTs. The larger inter-quartile range box for the group 2 is due to the only one net (G2.5) which results in 26% increase of resistance after the 200 TCTs.

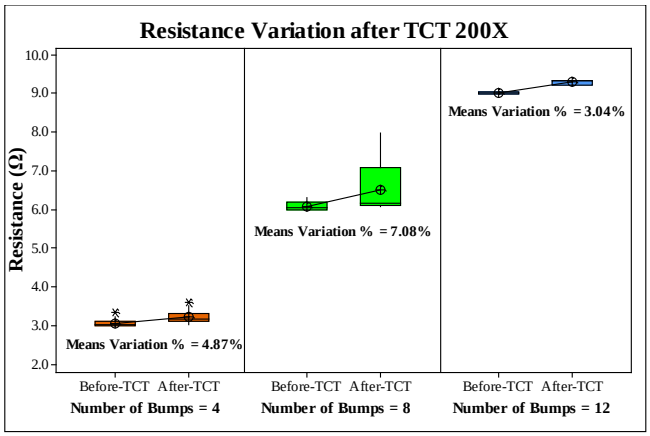

Figure 17 the means variation of the resistances for all groups before and after the 200 TCTs.

VII. Conclusion

The design of the glass substrate with TGVs is described in this paper as well as a mechanical test die for the assembly of SiP modules. The copper conductor of TGV is directly deposited and plated on the wall of through via as well as on the glass surfaces of both sides. After the assembly of SiP modules, daisy-chain open/short of RDLs are measured for the failure inspection of RDL and micro bump connections. The failures are mostly found at the locations between micro bumps of the test die and substrate RDL contact pads. This failure is mostly due to the uneven surface of nickel plated bonding pad. Detailed analysis of the failure will be continued with SEM inspections.

TCT reliability test result also has been reported in this paper. The reliability results are analyzed by comparing the daisy-chain electrical resistance before and after the 200 TCTs. The TCT results show that the variations of electrical resistance are within 10% for 24 out of the 25 daisy chains. Only one daisy chain result in 26% increase of resistance. Further TCT reliability is continuing for the sample #2 to reach the 500 TCTs.

Acknowledgment

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References

[1] Aric Shorey, et al., “Advancements in Fabrication of Glass Interposer”, Proceedings of 64th Electronic Components and Technology Conference, 2014.

[2] Dyi-Chung Hu, “Glass Technology and Manufacture Readiness” Invited talk, 5th Annual Global Interposer Technology Workshop at GIT, 2015.

[3] Yu-Hua Chen, Dyi-Chung Hu and Tzvy-Jang Tseng “20″ X 20″ Panel Size Glass Substrate Manufacturing for 2.5D SiP Application”, Proceedings of 65th Electronic Components & Technology Conference, 2015.

[4] Naoyuki Koizumi, “Basic Study of Packaging Structure Using Glass Material”, 4th Annual Global Interposer Technology Workshop at GIT, 2013.

[5] Vijay Sukumaran, et al., “Through-package-via Formation and Metallization of Glass Interposer”, Proceedings of 61st Electronic Components & Technology Conference, 2011.