Electrical Analysis and Modeling of 3D Through-Strata-Vias (TSVs) and Pads

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Abstract

Through-strata-via (TSV) is one of the most attractive3D integration solutions in that it offers a massive number of short interstrata connects, high data bandwidth, reduced delay and power consumption, small footprint, improved yield, heterogeneous integration and reduced volume-production cost. This work attempts to investigate the TSV signal integrity and, particularly, compares the performance among different TSV and pad combinations. Transient analysis, eye diagram and bathtub curves show a good behavior of TSV signal integrity in the time domain. Regarding to frequency response, the set of circular TSV and circular pad offers a slightly better performance than other shapes. When a misalignment is so large that the TSV does not land completely within the pad, the TSV frequency response is affected considerably. A big pad size degrades performance and decreases trace density, while a thinner pad would enhance process throughput and reduce cost. Simulation results also indicate that rather than using multiple small TSVs connecting to a common pad, it is better to implement one single big TSV because of less parasitics and coupling. Furthermore, the TSV component is carefully modeled, and the results from electromagnetic simulation and a broadband SPICE model are in a very good agreement.

Keywords: 3D; Through-strata-via (TSV); Pads; Electrical Modeling

1. INTRODUCTION

Apparently, scaling cannot continue forever because transistor dimensions are approaching atomic size. Since planar ICs encountered physical, technological, and economic limitations, 3D integration becomes a viable approach to alleviate such bottlenecks; a so-called "More than Moore" era has been coming. 3D integration is to stack functional blocks and connect them vertically [1]. In such a 3D system, signals travel vertically to device strata through short interconnects like bonding wires, flip-chip solder balls, and through-strata-vias (TSVs). In comparison to the inherent drawbacks of bonding wires and flip-chip solder balls, TSV emerges as a promising, probably ultimate way for 3D integration. TSVs offer the best of both system-on-chip (SoC) and system-in-package (SiP) for several reasons, including higher vertical density, improved performance, reduced power, higher fabrication robustness, lower cost and finally more functionality towards heterogeneous integration. TSV implementations are evolving from CMOS image sensor, DRAM stacks, memory on logic to heterogeneous integration [1]. This transition to true 3D integration requires smaller/denser TSVs, thinner substrates and faster time-to-market. It is critical to characterize TSV electrical performance.

Our previous work [2, 3] studied some impacts of TSV geometry on TSV electrical characteristics. As every TSV requires a pad for connecting the TSV to traces (i.e., planar interconnects), this paper focuses on the TSV configurations associated with pads using 3D electromagnetic (EM) solver Ansoft's HFSS, and provides some preliminary layout design guidelines.

2. TSV TRANSIENT CHARACTERISTICS

As shown in Fig. 1, we build a symmetric 3-layer stack-up composed of stratum 1's top dielectric layer (SiO_2, 2 μm), stratum 2's thinned substrate (Si, 30 μm), stratum 2's bottom dielectric layer (SiO_2, 2 μm) from bottom to top. Cu processing is assumed for forming the TSV and its pad; the pad dimension

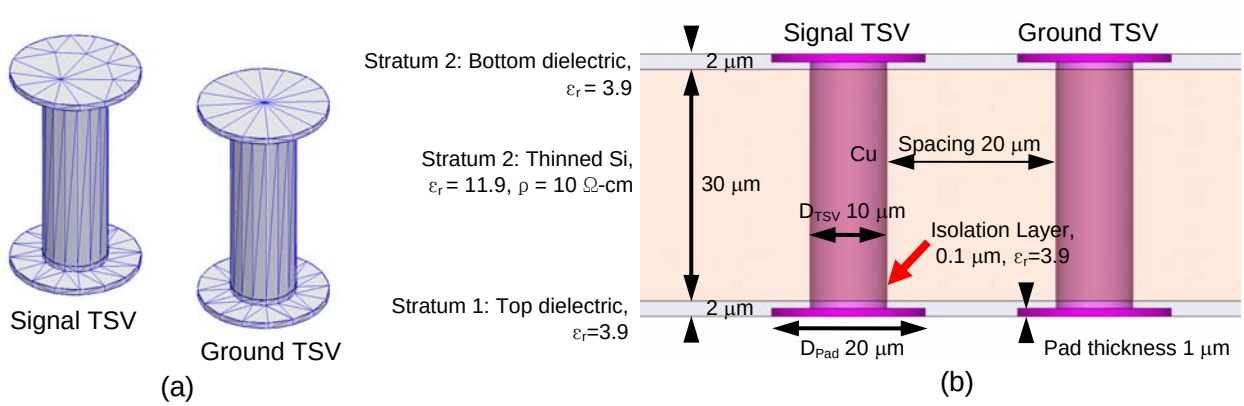

Fig. 1. Physical configuration of a signal-ground TSV pair, both TSV and pad are circular in shape. (a) Mesh, (b) Cross sectional view, this signal-ground pair structure serves as the baseline for TSV performance simulation throughout this work.

(D_{pad}) is twice the TSV dimension (D_{TSV}). Signal and ground TSVs have the same configurations in a pair, with a 20 μm TSV edge-to-edge spacing. A transient simulation of TSV is plotted in Fig. 2 for the voltages at input and output versus time. The pulse rise time is 35 ps and the period 1 ns. The input and output waveforms almost overlap; signal delay, ringing, and rise time degradation are rarely observed when a pulse

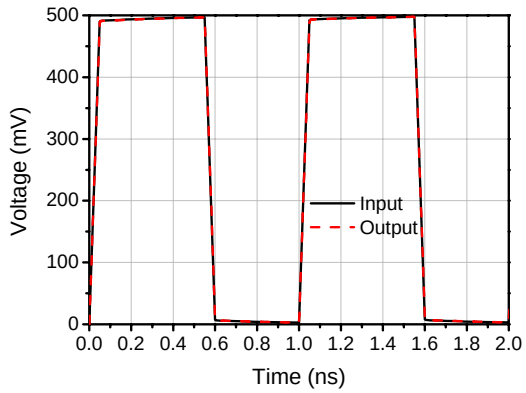

Fig. 2. Transient characteristics of TSV, input and output waveforms almost overlap. Signal propagation delay, ringing and rise time degradation are rarely observed.

travels along the TSV and its pads.

The eye diagram is to indicate the voltage and timing margins for distinguishing an individual bit at far end of a channel. In Fig. 3, the waveforms detected at the receiving end of TSV by transient analysis are overlaid at a unit interval; the color scalar represents the bit error rate (BER). The eye contour of 20 Gbps

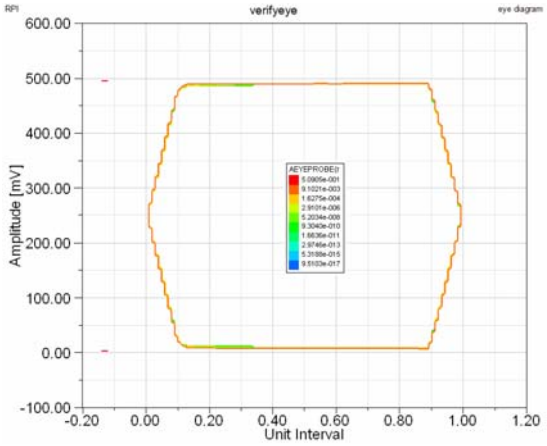

Fig. 3. The eye contour of 20 Gbps. The color represents the bit error rate (BER) at times within the unit interval. The wide and high eye opening indicates the good data quality preserved.

gives a fairly clean pattern representing little inter-symbol interference of the channel.

Another measure of signal integrity is the bathtub curve. In Fig. 4, horizontal and vertical bathtub plots show very low bit error rates at various locations of either timing in the unit interval or voltage transitions in the amplitude. The former uses the middle point of amplitude to measure the eye width and the latter holds the midpoint of unit interval to disclose the eye height. The small BER and jitter suggests a good signal quality under very high speed operations, thus, for the given TSV configuration, it is not needed to employ the techniques of feed forward equalization (FFE) or decision-feedback equalization (DFE).

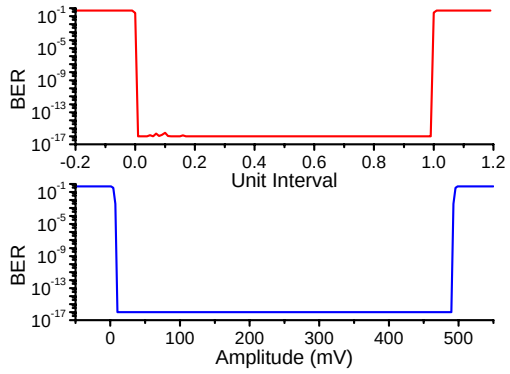

Fig. 4. The horizontal and vertical bathtub curves at 20 Gbps. The upper one shows the bit error rate (BER) at various locations of unit interval, while the lower one reflects BER along the amplitude range. Both graphics suggest TSV's very low BER.

3. TSV AND PAD IMPACT EVALUATION

In order to investigate the performance impact of the TSV and pad combinations, scattering parameters are simulated using finite element method (FEM) based Ansoft HFSS as a 3D field solver.

3.1 TSV and Pad Combinations

Four sets of TSV and pad configurations are selected; these configurations are based on the cross sectional shapes, i.e., circular or square. The cross sectional area is kept the same for all shapes; while the TSV edge-to-edge spacing is 20 µm. Results of scattering parameters S_{mn} are plotted in Fig. 5; corresponding return loss S_{11} and insertion loss S21 at 20 GHz are shown in Table I. As can be seen, for both TSV and pad, the shape impact on the performance based on S_{11} and S_{21} is not pronounced. Additionally, the circular shape has a smaller perimeter for the same cross sectional area, thus a reduced capacitance is expected. In comparison to the square shape, around 11% sidewall area reduction leads to a smaller fringe capacitance in the circular shape TSV and pad set; the circular shape set also contributes a smooth and small congregation of surface charge.

Table 1. S_{11} and S_{21} for different TSV and pad combinations at 20 GHz

TSV	Pad	S_{11}(dB)	S_{21}(dB)
Circular	Circular	-32.089	-0.195
Circular	Square	-32.217	-0.193
Square	Circular	-31.649	-0.200
Square	Square	-31.524	-0.201

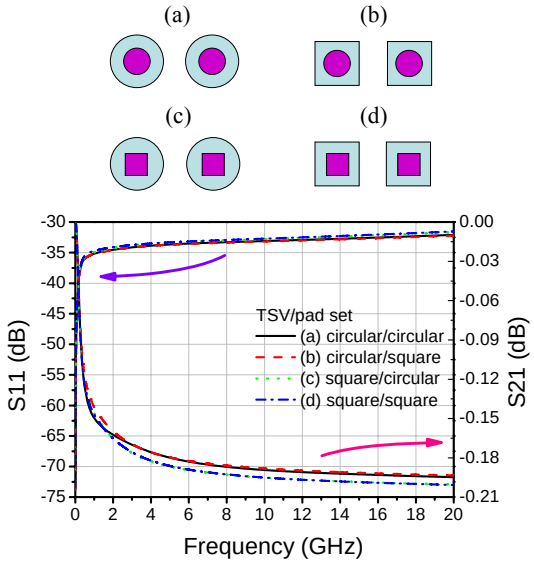

Fig. 5. Impact of TSV and pad sets in frequency domain, (a) circular pad and circular TSV, (b) square pad and circular TSV, (c) circular pad and square TSV, and (d) square pad and square TSV. Four combinations have the similar electrical performance, although the circular shape one is a little better.

3.2 TSV and Pad Offset

The sum of pad spacing and pad dimension is the pad pitch,

$$Pitch_{pad} = Spacing_{pad} + D_{pad}. \quad (1)$$

If a dual damascene process could be used, the TSV and its top pad could be formed simultaneously and well aligned using modern mask-alignment lithography technology. However, the misalignment between TSV and bottom pad (TSV landing pad) is in the range of microns because the bottom and top strata are aligned and bonded by chip-to-chip, chip-to-wafer or wafer-to-wafer approaches. A large pad can alleviate the high misalignment from the tools, at the expense of reduced TSV density. To ensure that the TSV lands on its pad, overlay accuracy (OA) of alignment and bonding needs to be conservatively included when designing a TSV pad,

$$D_{pad} = D_{TSV} + 2 \times OA. \quad (2)$$

In the case of chip-to-chip or chip-to-wafer, an overlay accuracy of 3-15 µm [4] is achieved today. Wafer-to-wafer alignment accuracy was demonstrated to be less than 1 µm [1, 4]. To give more process margin, D_{pad} (20 µm) and D_{TSV} (10 µm) are assigned in Fig. 1. The offset between TSV center

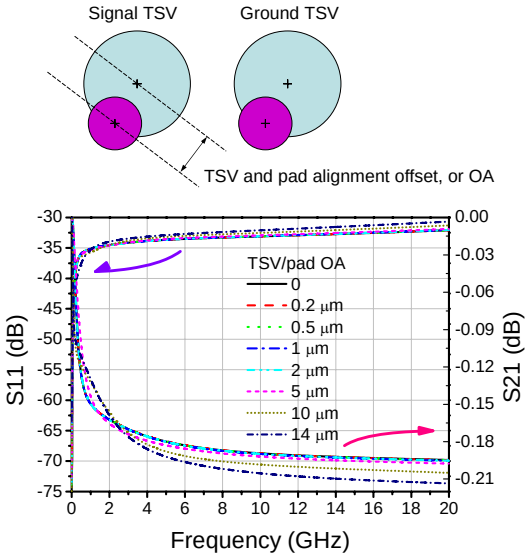

Fig. 6. Impact of TSV and pad offset in frequency domain. Shift between TSV and bottom landing pad engenders a poor electrical performance. An overlay accuracy (OA) within ± 5 μm does not affect S21 much, and S11 is slightly impaired.

and bottom pad center varies in a range of 0 μm to 14 μm. Simulated results in Fig. 6 suggest that so long as the TSV lands completely within the pad (i.e., the misalignment is <5 μm), the TSV performance remains almost the same. When a misalignment is so large that the TSV does not land completely within the pad, the TSV frequency response is affected considerably.

3.3 Pad Size and Thickness

Trace routing density is determined by TSV pad spacing in (1). Traces are desired to be squeezed through the space between the adjacent pads. Let "track" be the number of traces that could be inserted in between, and K_{pv} be

$$K_{pv} = \frac{D_{pad}}{D_{TSV}}. \quad (3)$$

The impact of K_{pv} on scattering parameters is shown in Fig. 7. We assume that bonding overlay accuracy (OA) does not violate alignment margin for this case, i.e.

$$OA \le \frac{(K_{pv} - 1)D_{TSV}}{2}. \quad (4)$$

When K_{pv} increases, S_{21} drops as a result of increasing parasitic capacitance. In addition, a large pad encroaches on the active space, resulting in fewer tracks and lower wiring density.

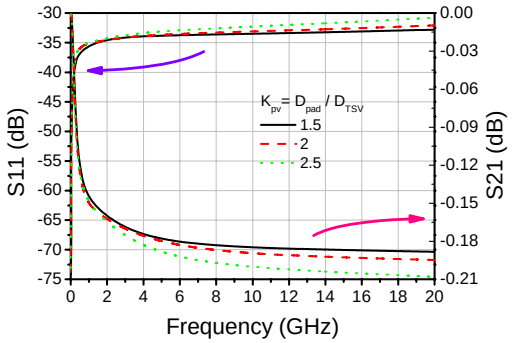

Fig. 7. Impact of pad size in frequency domain. Apparently, signal gain is reduced as the pad is enlarged that engenders more capacitance. Additionally, a large pad reduces the number of tracks.

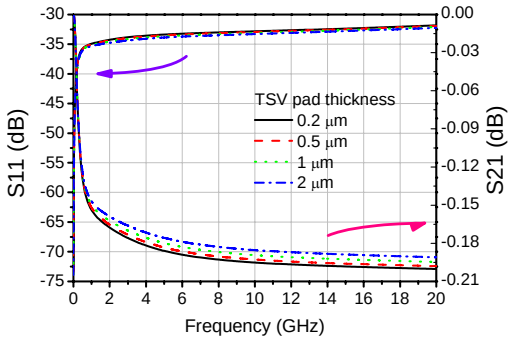

Fig. 8. Impact of pad thickness in frequency domain. The thicker pad improves a little.

Different pad thickness has been also considered as shown in Fig. 8. Although a thicker pad helps a little in performance improvement, it is recommended to use a thin pad without apparent performance degradation. A thin pad enhances fabrication throughput and reduces cost. Another advantage of a thin pad is that it slightly changes the current path in the vertical direction when there is a big offset between pads and TSV.

3.4 Pad Sharing by Multiple TSVs

In a comb structure, multiple TSVs might connect to a single pad, e.g., for signal/power/ground or redundancy. To simplify the analysis, the square TSV and circular pad set is selected because its performance is quite similar to that of circular TSV and circular pad (from Fig. 5). For four different schemes shown in Fig. 9, the total TSV area is kept the same. However, separated small TSVs almost double both AC resistance (due to skin effect at high

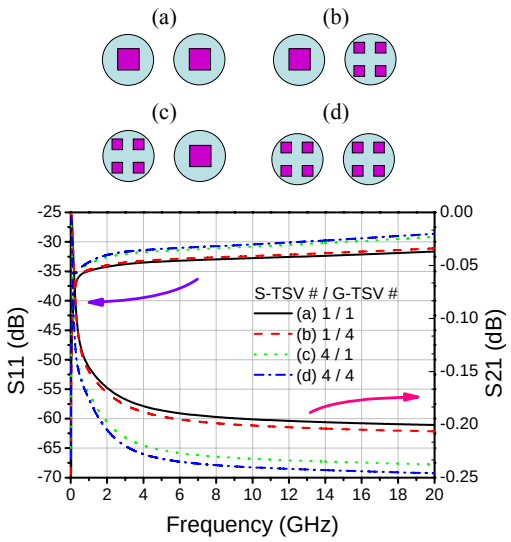

Fig. 9. Impact of multiple TSVs sharing a pad in frequency domain, (a) one signal TSV and one ground TSV (i.e., 1 S-TSV/1 G-TSV), (b) 1 S-TSV/4 G-TSVs, (c) 4 S-TSVs/1 G-TSV, and (d) 4 S-TSVs/4 G-TSVs. The results indicate that dividing a single big TSV into several small TSVs connecting to a common pad worsens the performance. Furthermore, the small TSV with a higher aspect ratio (HAR) may unfavorably hurdle the TSV fabrications.

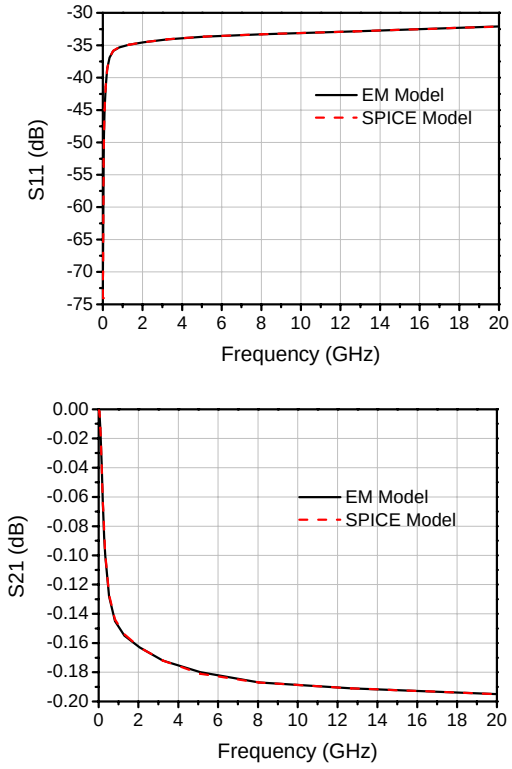

Fig. 10. Results of TSV SPICE model and EM solution in S11 and S21, which are in an excellent agreement.

speed operation) and capacitance (due to an extra isolation layer), leading to poorer performance. Since currents inside all small TSVs are in the same direction, mutual inductances are added, resulting in an increasing effective inductance. Furthermore, capacitive coupling among small TSVs contributes undesired parasitics to slow down the rise time and produce crosstalk noises. The configuration in Fig. 9a, i.e., a single big signal/ground TSV, has the smallest reflection noise and signal attenuation. The ones in Fig. 9b and 9c suggest that partitioning a signal TSV results in a worse S_{11} and S_{21} than a segmented ground TSV, and the one in Fig. 9d is the worst in that it has many explicit outgoing and returning current paths, all of which interact capacitively and inductively. In addition, etching and deposition of small and deep TSVs could be a technical barrier, depending on the TSV materials and processes.

4. TSV CIRCUIT MODELING

At present, in order to advance research and development of 3D integration, 3D EDA tools needs to support TSV. In this session, a TSV SPICE model is proposed for our structure in Fig. 1. Multiple voltage/current controlled sources are assembled at two TSV ports, generating a SPICE netlist whose scattering parameters match the electromagnetic solution. Fig. 10 shows the very good fitting results; the corresponding SPICE format file can be directly used in existing high-level simulators to evaluate the 3D systems and architectures using TSV technology. This approach helps save time and resources to characterize arbitrary TSVs using field solvers, facilitate and expedite the design cycle of 3D systems.

5. CONCULSION

As 3D TSV is regarded as the most promising solution in the “More than Moore” era, this work reports on electrical characteristics of TSV and pad in the time domain and frequency domain. Transient analysis, eye contour and bathtub curves show a good behavior of TSV signal integrity in the time domain. Different TSV and pad combinations are compared. The set of circular TSV and circular pad offers a slightly better performance. If the TSV lands

completely within the pad (i.e., the misalignment is <5 μm for the given TSV/pad configuration), the impact on TSV frequency response is small. This helps relax the 3D alignment demand to alignment tools. A big pad size degrades S_{11} and S_{21} and decreases trace density, while a thinner pad can improve throughput with little performance sacrifice. Instead of using multiple small TSVs sharing a common pad, it is better to implement one single big TSV. The frequency-dependent scattering parameters of TSV can be represented by equivalent circuit models, which can accurately capture TSV electromagnetic characteristics. This approach lends impetus to the development of infant 3D CAD tools.

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