ASM Pacific Technology

Multi Beam Full Cut Dicing of Thin Si IC wafers

Jeroen van Borkulo, Richard van der Stam, Won Chul Jung, Paul Verburg
ASMPT Laser Separation International B.V., platinawerf 20G, 6641TL Beuningen Netherlands

Abstract
Over the last years singulation of thin semiconductor wafers with (ultra) low-κ top layer has become a challenge in the production process of integrated circuits. The traditional blade dicing process is encountering serious yield issues. These issues can be addressed by applying a laser grooving process prior to the blade dicing, which is the process of reference nowadays. However, as the wafers are becoming thinner this process flow is not providing the yield and productivity required. In this article the unique ASMPT multi beam technology is presented which addresses both concerns and enables a high productivity laser dicing process with a limited heat affected zone and sufficient die strength.

Key words: 3D packaging, dicing, die strength, laser, thin wafer, multiple beam

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000474/2255907/isom-2015-wp52.pdf by guest on 29 November 2022

Introduction

For a long time the traditional separation technique used in this industry, i.e. blade dicing was able to fulfill the separation requirements of these wafers with a continuously increasing complexity. However, over the last 10 years it became clear that the requirements to process the advanced technology wafers in the semiconductor industry were very hard to follow for the blade dicing technique. We can distinguish two main areas where blade dicing encountered difficulties.

The first one is the transition from 2-D to 3-D IC-packages which requires thin wafers (<50um) to manage the heat dissipation and the geometrical size of the package. The mechanical forces from the blade dicing process pose a serious problem for those thin wafers. The combination of the thinner wafers with ultra low-k top layers does not allow customer to use the nowadays standard hybrid process of laser low-k grooving followed by a blade dicing process. Once Low-K grooved by laser the wafers are so thin that they will likely break prior to applying the blade dicing process. The semiconductor industry is still looking for a good solution which provides a high yield, high productivity and low cost dicing solution.

In the next sections a detailed explanation of the problem will be given. This is followed by the first results achieved for a single step, full cut process for thin Si wafers.

Alternative dicing technologies

To be able to find a solution for the dicing process of thin (ultra) low-K wafers alternative process steps have been developed. One of them is the so called Dice Before Grind (DBG). In the DBG process the wafer is partially diced while still at full thickness. In the subsequent process step the wafer is grinded down to the required thickness which separates the wafer.

Even though this technology is used in production nowadays it does so at the expense of yield loss (cracks and chipouts are observed, which results in unacceptable yield losses) and at the expense of cost. The cost is high due to the various process steps required (retaping, wafer handling, capex).

Another alternative separation technique similar to DBG is Stealth Before Grind (SBG). In this process flow a stealth process is applied prior to grinding the wafer which locally weakens the wafer. Once the grinding process has reached the required thickness the wafer can be separated via expansion of the tape. The constraints for this process flow is the cost of the equipment involved (specifically the stealth system) but as the dies are becoming smaller (<1mm), more and thicker TEG structures are used within the dicing street and wafers are getting thinner (<50um), an SBG process has difficulty to reach the required yield in combination with low cost.

Separation of thin (ultra) low-K wafers

As indicated in the previous section blade dicing is the standard technique to singulate a semiconductor wafer. In modern dicing machines the blade thickness can be reduced to 25 um, which in combination with an average IC-die-size of several square millimeters, has always tempered the need to go to an alternative separation technique. From a yield point of view the saw was meeting the specs

and the impact of the street width on the total number of die per wafer was low. This in contrast to, for example, the RFIC or LED industry where due to the smaller dies, street width reduction forms a significant die per wafer yield benefit. The laser dicing full cut process has become the process of reference in these segments with a utilization of >70% for RFIC and close to 50% for LED applications.
However, when the wafer technology approached the 65nm milestone, the use of low-k material instead of SiO_2 became inevitable, and the situation for die singulation changed drastically. Due to the brittleness and the relative poor adhesion between the silicon base material and the low-k layers the low-k layer delaminates and cracks when the mechanical force of the blade is applied. This results in a significant reduction of the dicing quality (*figure 1*) and yield problems.

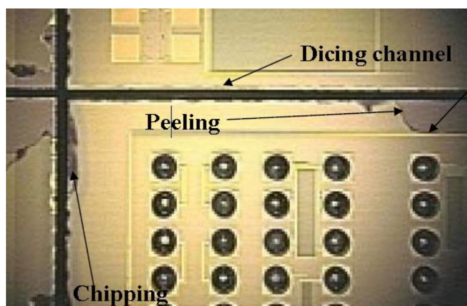


Figure 1: *Top view of a blade diced low-k wafer. Severe peeling, chipping is clearly visible.*

Laser full cut Si

As various studies have shown the die strength level for a standard laser full cut process tends to be 30-50% below the saw blade reference [1]. Despite that lower die strength level no yield issues were found during assembly process.
In order to improve the die strength for the laser dicing process additional process steps have been added to increase the die strength [2]. Even though these studies showed that it is possible to achieve die strength levels equal to the blade dicing process they did so with the aid of additional process steps (wet etch, dry etch). It is therefore impacting the cost and also the flexibility of the process.
The root cause for the low die strength for a standard laser dicing process is the combination of recast material (molten Si) and the formation of micro cracks along the surface interface (see figure 2 below).

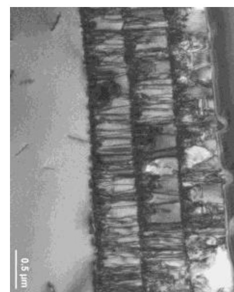


Figure 2: *TEM image of the recast interface of a laser diced 100um polished Si wafer.*

The interface of the crystalline Si and the amorphous recast material creates stress which when placed under pressure can initiate a crack and therefore lower die strength.
By means of etching processes (wet or dry) the recast material is removed and micro cracks generated at the Si recast interface are released of their stress.

Die strength

All results mentioned in this paper have been measured on a 4-point die strength tool both active Structure Up (SU) and Structure Down (SD) (see figure 3).

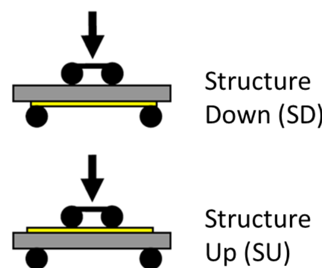
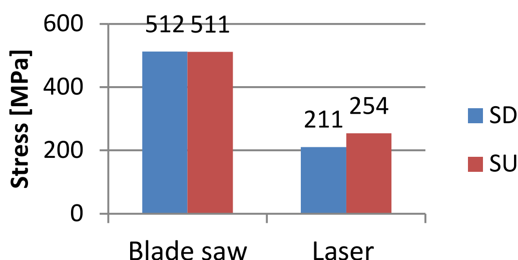


Figure 3: *SD and SU measurement method on 4-point bending tool.*

In the underneath graph 1 the die strength results are shown for a standard laser dicing process vs. a blade saw process. The wafer used for this test is a 70um polished Si wafer. For reference purposes the same wafer type has been blade diced.
The data shows clearly the reduction in die strength for a standard laser dicing process with respect to a blade dicing process. In the past various parameter changes to the laser dicing process have been applied (pulse duration, power, etc) however the result on the die strength improvement was marginal(<5%).

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000474/2255907/isom-2015-wp52.pdf by guest on 29 November 2022



Graph 1: *Die strength results Su & SD of a 70um polished Si wafer measured on a 4-point bending tool.*

Laser cleaning

It is found that when irradiating the dicing kerf with lower power pulses both the visual appearance and die strength of the die is significantly improved. For a standard laser dicing result on a 100um thick polished Si wafer (see figure 4) irregular and significant amount of recast material is visible which contributes to the lower die strength achieved with this process. When applying the laser cleaning process the recast formation is altered and can be reduced and smoothened at the same time (see figure 5).

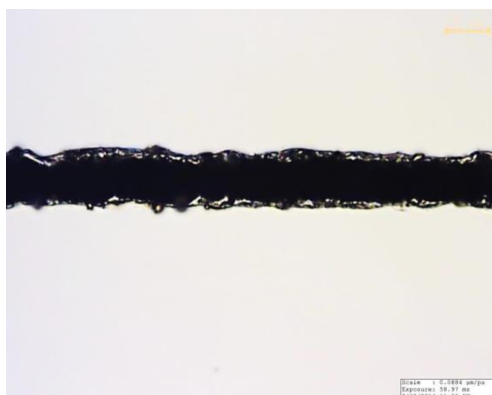


Figure 4: *Top view of a full cut laser diced 100um thick polished Si wafer. Abundant and irregular recast is clearly visible.*

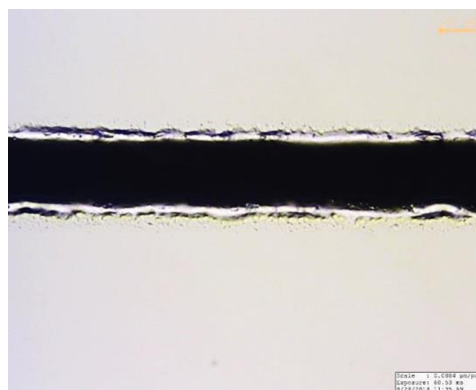


Figure 5: *Top view of a full cut laser diced 100um thick polished Si wafer which has been treated with a laser annealing process. Significant reduction of recast formation is visible and the remaining recast is smoother.*

Inspection of the side wall structure and roughness also demonstrates that the laser cleaned area has a smoother appearance (see figure 6 & 7 below). The result shown in figure 7 has only been treated for the top section of the side wall.

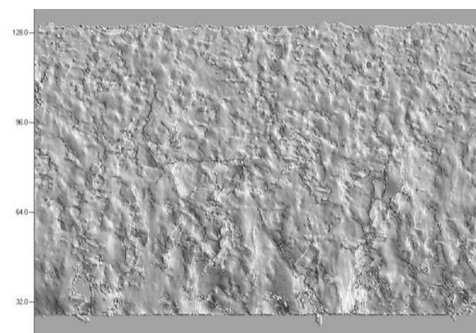


Figure 6: *Side wall quality of a standard laser dicing process.*

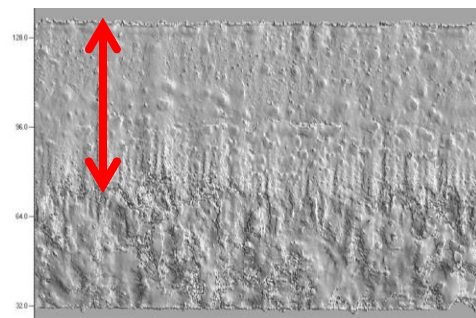


Figure 7: *Side wall quality of a top side laser cleaned die. The red arrow indicates the treated area. Clearly visible is the difference in surface structure.*

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000474/2255907/isom-2015-wp52.pdf by guest on 29 November 2022

V-Shape DOE

The standard full cut laser dicing process for ASMPT is done with a multi beam laser configuration where all beams are in line with the dicing direction. It was found that lower power beams running over the edge of the dicing kerf will help to clean up the recast and micro cracks and as a result recover the die strength. As the cleaning process is done on the edges of the laser diced area it would require additional process traverse with an offset to both sides of the edges of the dies to apply the cleaning process. This obviously reduces the productivity of the process. ASM Laser Separation International is the inventor of multi beam laser dicing and a multi beam configuration is developed which allows the cleaning process to be done in a single pass.

As shown in figure 8 below the V-Shape DOE (patent pending) consists out of centralized higher intensity beams which dice the wafer and outer lower intensity beams which take care of the cleaning process.

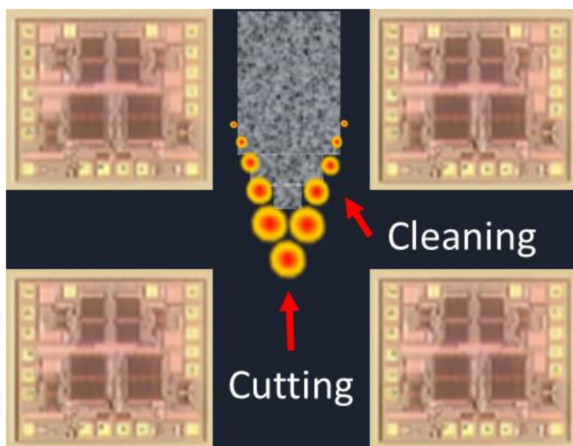


Figure 8: *V-Shape DOE design showing the central forward positioned spots which are used to dice through the wafer and the outer lower intensity spots which clean the edges of the die.*

The V-shape DOE design enables a single process full cut thin Si laser dicing process with a sufficient die strength.

As no additional equipment is required as well as no additional process steps (e.g. retaping, extra wafer handling, etc.) the cost of ownership of this process will be competitive.

V-DOE Results

Demonstrated below in figure 9 is the result of dicing through a 75um thick polished Si wafer which was taped on a 20um DAF tape. Figure 9 shows the side wall quality of the cut demonstrating that the V-DOE process has diced through the Si and the DAF tape and that the top section of the side wall has been cleaned.

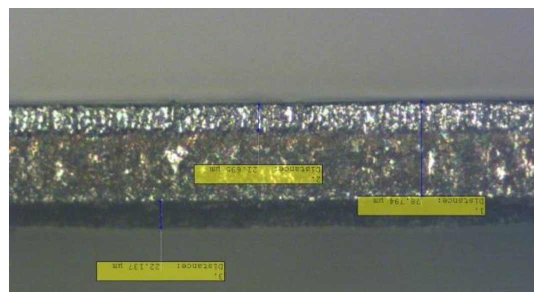


Figure 9: *Side wall of a 75um thick polished Si wafer on 20um DAF. The top section of the side wall is clearly cleaned and recast material removed.*

In figure 10 the top surface dicing quality is shown using a V-DOE process to dice through a 65um thick NAND Flash memory device mounted on 20um DAF. The die size for this wafer is 8800x10370um and a productivity of 8WPH is achieved.

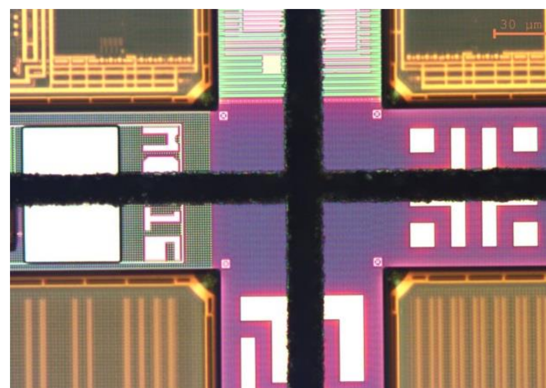
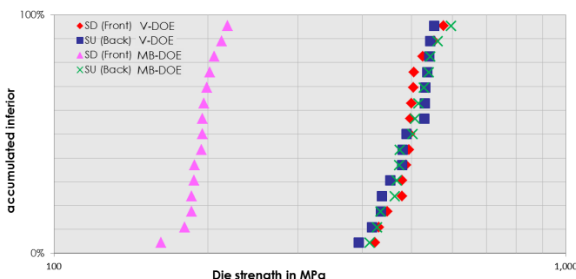


Figure 10: *Top surface quality achieved on NAND Flash memory device 65um thick on 20um DAF. Dicing width 20um.*

The die strength results demonstrated in graph 2 and table 1 below for a V-DOE process is showing a 100% die strength improvement with respect to a standard laser dicing process and is therefore similar as the blade dicing process. The results have been achieved on various wafer thickness and DAF tapes

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000474/2255907/isom-2015-wp52.pdf by guest on 29 November 2022

but also on various products wafers with and without DAF. Shown in below is the result for only one condition.
The purple points in the graph below show the SD die strength results for a standard laser dicing process. The red points in the graph below show the SD die strength result for the V-DOE process. The die strength for SU situation is already high due to the dicing parameters chosen for the dice through process. Therefore the cleaning is only required on the top side of the die side wall.



Graph 2: *Die strength results SU & SD and for standard Multi Beam (MB) laser dicing process and V-DOE process for a 75um Si wafer on 20um DAF measured on a 4-point bending tool.*

	V-DOE Dicing		MB-Dicing	
	Front side	Back side	Front side	Back side
Average (Mpa)	493.2	490.1	193.9	496.3
5% lower bound	412.2	385.9	166.5	391.9
SD (Mpa)	40.5	52.1	13.7	52.2

Table 1: *Die strength results SU & SD for standard MB laser dicing process and V-DOE process for a 75um Si wafer on 20um DAF measured on a 4-point bending tool.*

Conclusions

Both the thinning of wafers for 3D stacking and the use of ultra-low-k materials means that the semiconductor IC industry is looking at alternative technologies to separate their wafers.
The V-DOE concept of ASMPT shows that die strength levels can be achieved equal to the blade dicing process which is considered the reference nowadays. The results show that the combined laser dicing and cleaning process allows a high dicing quality in combination with die strengths levels for both SD and SU between 400MPa to 550MPa. Deployment of the technology is currently ongoing with evaluations done together with major players within the semiconductor industry.

Reference

[1] DoHyung Kim, "Evaluation for UV Laser Dicing Process and its Reliability for Various Design of Stack Chip Scale Package", 58th ECTC 2009, pp 1531-1536
[2] Jianhua Li, “Laser Dicing and Subsequent Die Strength Enhancement Technologies For Ultra-thin wafer”, 57th ECTC 2007, pp 761-766.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000474/2255907/isom-2015-wp52.pdf by guest on 29 November 2022

ASM Pacific Technology
ASM Laser Separation International (ALSI) B.V.
Platinawerf 20G, 6641 TL Beuningen, The Netherlands
Tel: + 31 (0)24 678 28 88
Fax: +31 (0)24 678 28 99