# Biocompatible encapsulation and interconnection technology for implantable electronic devices

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## Abstract

*A biocompatible packaging process for implantable electronic systems is under development at imec, combining biocompatibility, hermeticity, extreme miniaturization and cost aspects.*
*In a first phase of this packaging sequence, hermetic chip sealing is performed by encapsulating all chips to realize a bi-directional diffusion barrier preventing body fluids to leach into the package causing corrosion, and preventing IC materials such as Cu to diffuse into the body, causing various adverse effects. For cost effectiveness, this chip sealing is performed as post-processing at wafer level, using modifications of standard clean room (CR) fabrication techniques. Well known conductive and insulating CR materials are investigated with respect to their biocompatibility, biostability, diffusion barrier properties and sensitivity to corrosion. Material selection and integration aspects are modified until good properties are obtained.*
*In a second phase of the packaging process, all chips of the final device should be electrically connected, applying a biocompatible metallization scheme. We selected the use of Pt due to its excellent biocompatibility and corrosion resistance. Since Pt is very expensive, a cost effective Pt-selective plating process is developed.*
*During the third packaging step, all system components such as electronics, passives, a battery,... will be interconnected. To provide sufficient mechanical support, all components are finally embedded using a medical grade elastomer such as PDMS or Poly-urethane.*

Key words: implantable packaging, biomedical device, biocompatibility, hermeticity, corrosion resistance, platinum metallization.

## INTRODUCTION

Implantable electronic devices such as pacemakers are typically packaged in a rigid Titanium (Ti) box to ensure hermetic and biocompatible packaging of the microelectronic device. Such a Ti-box is a well-known and safe package for implants. On the other hand, the Ti box is often large compared to the electronics inside, hence during implantation a larger insertion wound is needed resulting in a more pronounced Foreign Body Reaction (FBR) and a higher infection risk upon implantation. Also chronic adverse effects such as irritation are more likely due to the strong mismatch between the soft body tissue and the rigid Ti-box [1,2].

In this work, miniaturization trends in packaging of microelectronics will be extended towards packaging of implanted electronic devices. Moreover, by selecting the proper materials, the final package can be made soft and biomimetic, resulting in a comfortable implantable device and reducing the risk on pronounced FBR and adverse effects.

## PACKAGING CONCEPT

The concept of this implantable package is illustrated in Fig. 1. Three main phases are distinguished:
- Phase 1: chip encapsulation
- Phase 2: fabrication of subsystem package /interposer
- Phase 3: final system assembly and embedding

In the **first phase**, individual dies (or subdevices) are encapsulated by one or more capping layers in order to provide a hermetical enclosure for each die. The encapsulation consists preferably of a stack of layers, to ensure hermeticity by avoiding any influence of possible pinholes. The die encapsulation layers should fulfill the task of bi-directional diffusion barrier: no body fluid should leach into the device, and harmful IC materials such as Copper (Cu) should not diffuse into the body tissue. Obviously the capping layers should also be biocompatible, which means that the material should not cause harm to the body. Biocompatibility is a contextual concept, hence depending on duration and type of body contact, and depending on the implant location, more stringent demands are imposed on the material to avoid any harm. We will focus in this publication on a long term subcutanious implant (implantation longer than 30 days).

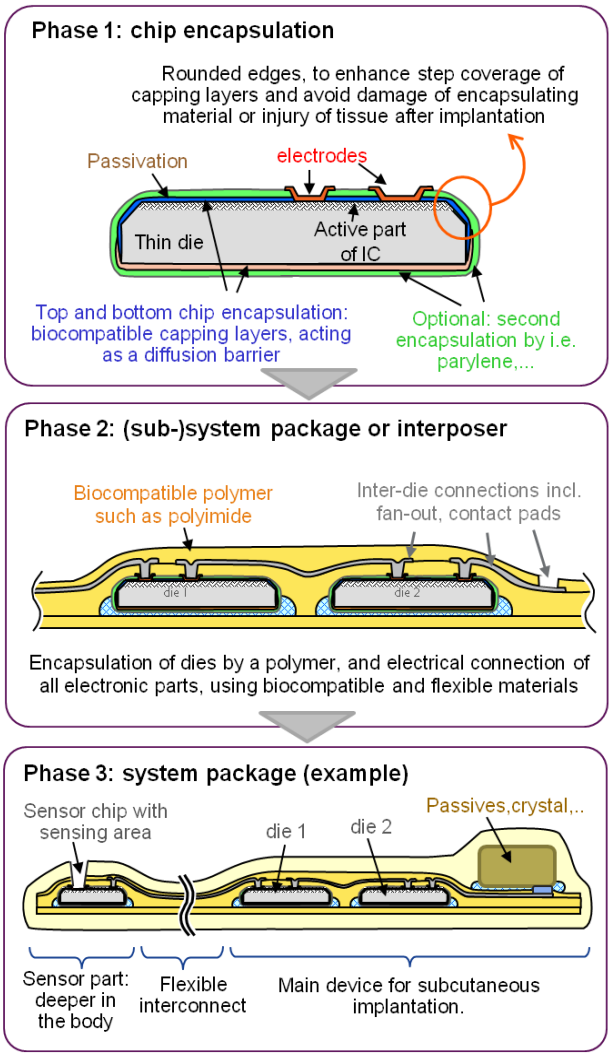


***Fig. 1.*** *proposal for a compact implantable packaging (1) all chips are individually encapsulated by diffusion barriers using a wafer level process; (2) biocompatible chip interconnect and embedding of multiple chips by a supporting flexible polymer such as polyimide; (3) final system assembly including biocompatible metallization and final embedding, preferably in a soft biomimetic polymer.*

In a **second phase** of the packaging process, all chips of the final device will be placed on a common carrier, which is preferably a thin flexible film giving sufficient support. Medical grade polyimide is an interesting insulating carrier material due to its mechanical strength and its barrier properties. The chips are also covered with a protective layer, again polyimide is interesting as insulating barrier material. Finally the chips will be electrically connected, by applying a biocompatible metallization scheme using for example gold (Au) or platinum (Pt), which are interesting biocompatible metals for implants due to their high corrosion resistance. For electrodes being in direct contact with the tissue after implantation, improved performance is expected when locally the Au or Pt is covered by IrOx.

During the **third phase** and final packaging step, all system components such as electronics, passives, a battery,... will be assembled and interconnected. To provide sufficient mechanical support to all components, an embedding is essential, preferably using a soft, flexible material which will reduce the body reaction upon implantation due to the materials biomimetic nature (flex, soft material cfr. tissue). Biocompatible elastomers such as medical grade polyurethane or PDMS are interesting candidates.

## FABRICATION OF THE DIE ENCAPSULATION

A dedicated process is developed for the chip encapsulation in phase 1 of this packaging approach. This process is described in more detail in previous publications [3,4], hence only a short summary is given below. Phase 1 is carried out as wafer-based post-processing in the clean room (CR), hence many chips are processed simultaneously, reducing the cost of this process step.

After standard IC processing, front side partial dicing is performed (~100µm dicing depth), to allow for further full wafer processing. The partial dicing is followed by die rounding to realize a slope at the top of the groove, which is essential to obtain a good step coverage of the barrier layers. After this sloped dicing, the top and sidewalls of the chip are simultaneously covered with a stack of barrier layers to form a bi-directional diffusion barrier. Dedicated deposition processes are developed to obtain good step coverage at max. 400°C, essential to maintain chip functionality. Good step coverage is crucial to ensure good barrier properties of the chip encapsulation. For the subsequent backside encapsulation, the whole wafer is temporary glued upside down on a carrier wafer and the wafer is thinned down to ~50µm. Next all chips are

covered at the backside and sidewalls with the backside barrier layers. The temporary adhesive used during this process step, is not stable above 200°C, hence the bottom barrier layers are deposited at a temperature of 200°C max.

### DIFFUSION BARRIER MATERIALS: GENERAL CONSIDERATIONS

The capping materials used for die encapsulation should be biocompatible and should serve as suitable bi-directional diffusion barrier. Furthermore, the materials need to be bio-stable: they should not change when exposed for a very long time period to body fluids. With respect to electrical properties, two types of materials needs to be identified: insulating barriers and barriers which are conductive to fabricate the electrical contacts, as shown in Fig 2.

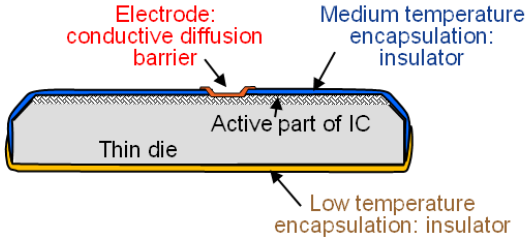


***Fig. 2 :*** *Cross-section of an encapsulated chip. The top and bottom encapsulation layers form an insulating diffusion barrier, the interconnection electrode needs to be a conductive diffusion barrier. All these diffusion barriers consist typically of a stack of various layers.*

### *A. Biocompatibility tests*

The first step in biocompatibility testing consists of cytotoxicity tests. In this work these tests are performed according to the ISO 10993-5 standard regarding biocompatibility. Cell cultures from primary neonatal mouse cardiomyocytes are used. The test procedure is schematically shown in Fig. 3. Details about the applied cytotoxicity tests can be found in Ref. [4].

### *B. Diffusion tests*

For this test, Cu is chosen as test vehicle since it is commonly present in chips and since it is known to diffuse fast. Furthermore, Cu diffusion into a cell culture will be detected easy since Cu is (highly) toxic for most cells [5].

Two types of tests are needed for diffusion characterization of barrier layers:

(1) test of diffusion of Cu through the barrier layer, done by Cu sensitive cell cultures. This test procedure is schematically shown in Fig. 3.

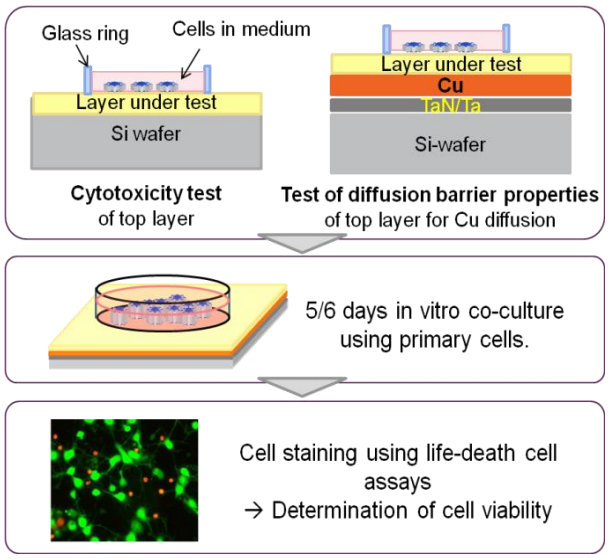


***Fig 3:*** *Test protocol for cytotoxicity tests and diffusion barrier tests*

(2) evaluation of fluid leaching through the barrier layer into the chip, done by Cu corrosion tests during/after submersion.

Details about the applied diffusion tests can also be found in Ref [4].

### *C. Accelerated diffusion tests*

Diffusion evaluation based on cell co-culture tests is typically limited to a duration of 5-6 days, since a longer test period will often result in cell death due to overpopulation or to aging of the medium. This short test period is in contrast with the use of long term implants. Hence accelerated testing with respect to bi-directional barrier properties is essential. For electronics, accelerated diffusion testing is typically done using elevated temperatures. Diffusion and corresponding Mean Time To Failure (MTTF) are related to time and temperature, as expressed in the well known Arrhenius equation [6]:

$$MTTF = A\exp(-\frac{Ea}{kT})$$

With: A : pre-exponential constant
Ea : activation energy
T : temperature in Kelvin
k : Boltzmann's Constant

A conservative estimate of accelerated aging factor for corrosion is the following: 3 days at 70ºC is equal to 1 months at 37ºC ($Q_{10}$=2). But the activation energy for humidity induced corrosion in semiconductor devices is 0.8-1 eV. Hence, assuming Ea=1eV, 3 days at 70ºC corresponds to ~5 months at 37ºC ($Q_{10}$=3.8). An accurate prediction of the acceleration factor needs always device specific calibrations.

Note that it is useless to perform cell cultures at elevated temperatures to accelerate diffusion: incubation at temperatures above 45-50°C results in denaturization of proteins in the cells and in the medium, resulting in cell death.

Elution tests can also be used to evaluate diffusion, and such tests offer better possibilities related to accelerated testing. For an accelerated elution test, a biofluid is exposed several days to the material under test at an elevated temperature. We perform such tests at 70°C, the high temperature elution condition according to the USP standard. After the elution period, the biofluid can be analyzed, to check if traces of Cu can be found, eg. based on TXRF analysis [5].

### *D. Bio-stability tests*

Biostability of the barrier materials is evaluated by immersing the films for a long period in Di-water and/or various biofluids such as Phosphate Buffer Saline (PBS) which is simulating blood serum, and cardiomyocyte culture medium which is simulating cardiac tissue fluid. Real-time biostability tests are performed at 37°C for a duration of several weeks, while accelerated testing is performed at 70°C for typically 1 to 2 weeks.

## INSULATING DIFFUSION BARRIER MATERIALS: CHARACTERIZATION

The insulating capping layers can be composed of silicon oxide (SiO2) and nitride (SiNx), two well-known passivation materials in a standard CMOS CR. We investigated SiO2 and SiNx deposited at ~400°C (front side capping) and ~200°C (backside capping). Based on primary cell cultures performed according to the ISO 10993-5 standard regarding biocompatibility, we proved that our materials are non-cytotoxic. Diffusion tests revealed that the SiO2 and SiNx films deposited at 400°C have better barrier properties to stop copper diffusion compared to the films deposited at 200°C. Details about the biocompatibility and diffusion tests results for these materials can be found in Ref. [4].

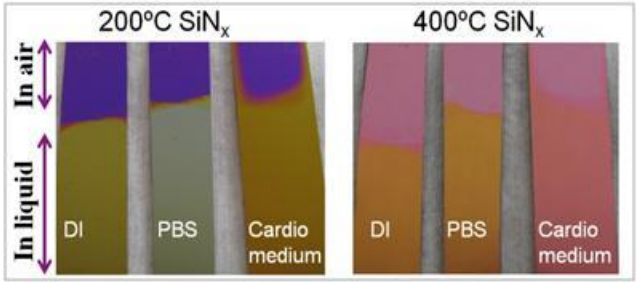


***Fig 4:*** *$SiN_x$ after 4-week incubation in DI-water and bio related fluids at 37°C. Top parts were only exposed to air. Left are PECVD $SiN_x$ samples deposited at 200°C and the samples at the right are deposited at 400°C.*

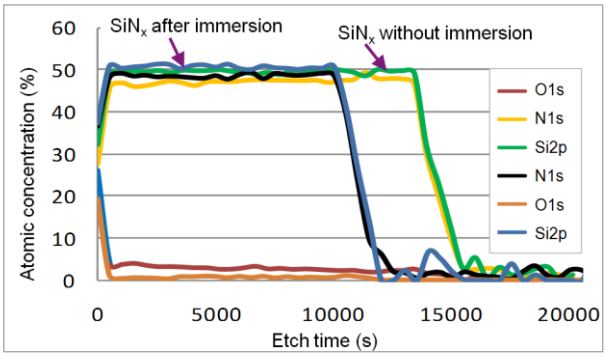


***Fig 5:*** *XPS analysis of $SiN_x$ film before and after 2 weeks immersion in 70°C DI water.*

Biostability of the SiO2 and SiNx films is evaluated by immersing the films for 4 weeks in DI-water and various biofluids such as PBS and cardiomyocyte culture medium. Real-time biostability tests at 37°C are performed for a duration of 4 weeks. The SiO2 layers remained stable, but a clear color change of SiNx occured, as illustrated in Fig 4.

Accelerated tests at 70°C showed the same color changes but they occurred faster compared to real time biostability tests. In order to understand this color change, the samples are analyzed with FTIR and XPS techniques before and after immersion. The FTIR spectrum showed no change in absorption peaks due to immersion, which is proving that the chemical composition of the SiNx film is not changing during immersion. With an XPS analysis (Fig 5), the atomic concentration of various elements is evaluated during etching of the sample under test. For the immersed SiNx sample, a shorter etch time of the SiNx layer is observed, while the atomic concentrations of the samples before and after immersion are the same, showing that the SiNx layer gets thinner by immersion. This leads to the conclusion that the SiNx film is dissolving in the DI water. This conclusion is remarkable, since SiNx is used regularly in standard CMOS processing, but for CMOS a rinse in DI-water is always short, while for long term implant applications long immersion tests should be done.

Obviously, this dissolution of the SiNx layer in water and biofluids is not acceptable for implant applications, hence the problem needs to be understood and solved. In literature, a linear relation is reported between the etch rate of SiNx in buffered HF, and the H-concentration in the SiNx layer [7]. Based on this knowledge, we tested 3 types of SiNx regarding to their stability in DI-water and PBS:

- PECVD SiNx deposited at 200°C (H content 20-25%)
- PECVD SiNx deposited at 400°C (H content ~15%)
- LPCVD SiNx (H content only ~3%)

The hydrogen content in the SiNx films is determined using Elastic Recoil Detection .

All SiNx types are immersed in DI water and PBS at 70°C for 1 week. Also in our tests, the dissolution rate of the SiNx samples was proportional to the H content, due to the influence of H content on the SiNx film structure. Even the LPCVD SiNx layer with lowest H content showed a clear color change after only 1 week immersion at 70°C (DI-water). Hence SiNx cannot be used as the top layer of the die encapsulation for an implantable device, if moisture can penetrate down to this layer after implantation.

To solve the problem created by the instability of SiNx in biofluids, we evaluated also the biostability of silicon carbide (SiC) deposited at 350°C, using the same immersion conditions as for SiNx tests. The SiC layer proved to be stable in 70°C DI water and in PBS for at least 3 weeks, corresponding to at least ~6 months stability at 37°C (See Fig. 6). Also cytotoxicity tests were performed for SiC, with very good results. Hence for chip encapsulation, SiC will always be deposited on top of SiNx to ensure good biostability.

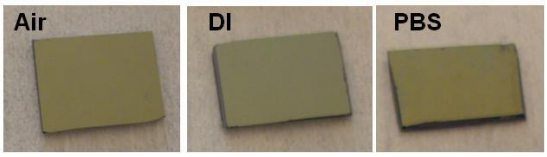


***Fig. 6:*** *SiC after 3 weeks incubation in DI-water and in PBS both at 70°C.The SiC layers are very stable. (SiC: 50 nm thick layers deposited at 400ºC)*

### CONDUCTIVE BARRIER MATERIALS: MATERIAL SELECTION

For the fabrication of the conductive barrier stack, again well-known clean room materials are selected: titanium (Ti), Ti-nitride (TiN), tantalum (Ta) and Ta-nitride (TaN). Depending on the deposition process conditions these materials will be biocompatible and can have interesting barrier properties, as reported in literature [2,8,9]. Certain noble metals such as Au and Pt are very interesting materials for biomedical applications, but these materials they might deteriorate the standard IC processes due to cross contamination. Hence for Phase 1 of our packaging concept, consisting of wafer level based processes carried out in the clean room, Au and Pt are not suitable as conductive barrier materials. Phase 2 and 3 of this packaging concept will take place in a laboratory (packaging house) hence outside the clean room, therefore in these packaging phases noble metals such as Au and Pt are considered (see further).

### CONDUCTIVE BARRIER MATERIALS: CHARACTERIZATION

As conductive barrier layers for phase 1, Ti, TiN, Ta and TaN are tested. For each of these materials, a thickness of ~100nm is deposited for these tests.

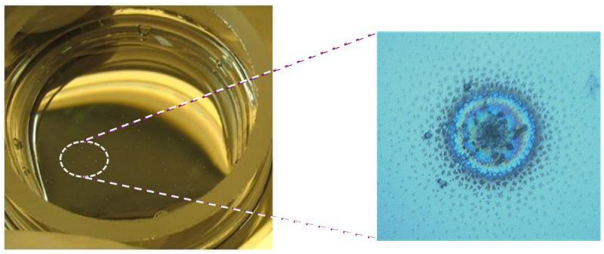

***Fig. 7:*** *TaN after immersion in PBS at 37ºC for 10 days. Pitting is clearly visible after 10 days already.*

The cytotoxicity test results are very good for all 4 materials. With respect to diffusion barrier properties, we can conclude that ~100nm Ta is not performing well at all, and 100nm TiN has better but still marginal barrier properties. TiN layers might be a sufficient barrier if layers are used which are considerably thicker than 100nm. Ti and TaN are performing very well as barrier under the test conditions. Details about the biocompatibility and diffusion tests results for these materials can be found in Ref. [4].

Long term biostability tests are performed with Ti, TiN, Ta and TaN. The materials are immersed in Cardio cell culture medium, in Dulbecco's Modified Eagle Medium (DMEM) and in PBS all at 37ºC for 4 weeks. Immersion in PBS resulted in clear pitting for all materials (See Fig. 7), while the same materials performed very stable in both other bio-fluids.

To ensure stability in all bio environments, it was decided to cover always the conductive barrier stack with a noble metal such as Platinum (Pt) to be on the safe side for all applications. Pt is not compatible with standard CMOS processing, but the Pt deposition and lift-off etch can be done outside the clean room, since it is the last step in the process sequence of phase 1 before further packaging.

### CORROSION TESTS PERFORMED ON A DEDICATED TEST DEVICE

As mentioned before, the encapsulation of phase 1 should form a bidirectional diffusion barrier, to protect the body for the implanted electronics and the electronics for corrosion by body fluids. We fabricated a corrosion test device carrying long copper interconnects on chip, using the encapsulation processes as mentioned before and illustrated in Fig. 8. Since the bondpads/electrodes are the most sensitive features for moisture diffusion (see red arrow in Fig 8), extra bondpads/electrodes are added to the Cu interconnects of the test device to create a worst case scenario for corrosion. The Cu interconnects are fabricated using a damascene process, interconnects with various line widths (500nm to 50µm) are present on the test device. For electrode fabrication, the contact pads are covered with a barrier stack consisting

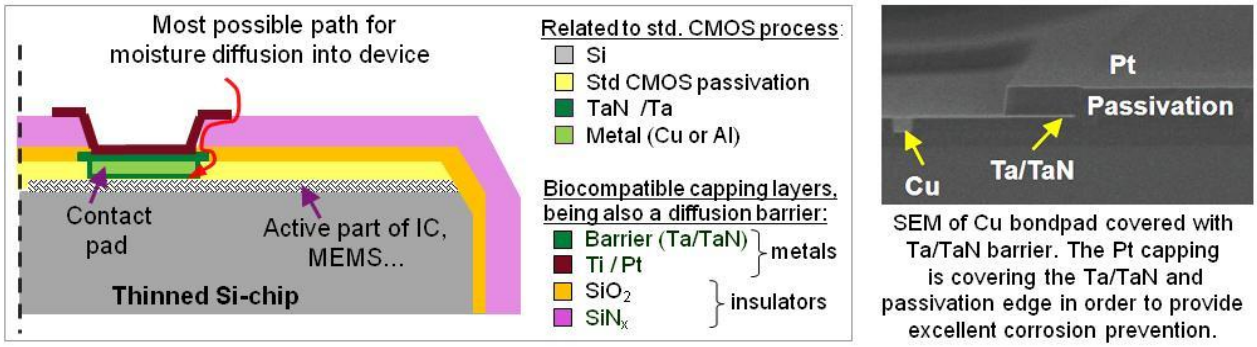


***Fig 8:*** *Left: schematic of the corrosion test device; right: SEM photo of contact pad*

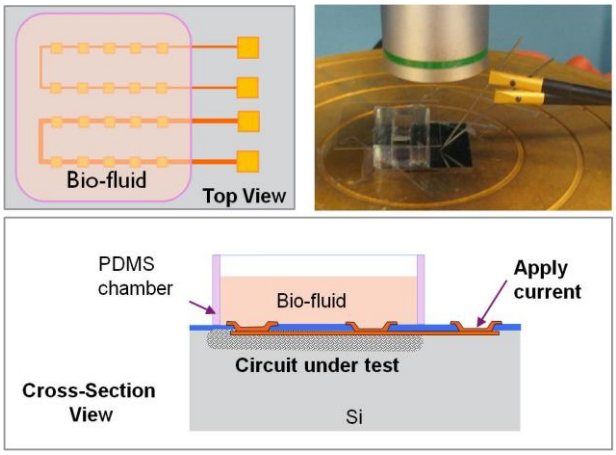


***Fig 9:*** *Active corrosion test setup. Left and bottom: schematic top and cross-section view; Right: photo of the device under test. A PDMS ring glued on the device enables selective immersion of the electrodes.*

of 40nm TaN on top of 15nm Ta, and for biostability reasons this stack is covered with an extra layer of 50nm Pt. The Pt layer is covering also the edges of the passivation layers to ensure very good protection of the TaN bondpad cap (see structure in Fig. 8).

Passive accelerated tests are carried out by immersion of the corrosion test device in PBS at 70°C up to 2 months. 4-point resistance measurement are carried out at regular time intervals for interconnects with a linewidth of 1µm, 5µm, 10µm and 40µm. For all these structures, no resist change is observed nor other corrosion effects were visible. This result is very good, since 4 weeks incubation at 70°C corresponds to ~2 years stability against corrosion at 37°C (assuming $Q_{10}$=2 in the Arrhenius equation) .

In active tests, the device is immersed in PBS except for the main contact pads needed for the external connections at which 1 mA AC or DC current is applied (see Fig. 9). Meanwhile the voltage across the device is monitored. So far the devices have proven to be corrosion-free for 2 weeks under this test condition. Accelerated active corrosion tests are ongoing by immersion of the device in PBS at 70°C. The test device has proven to be resistant to corrosion under 0.1mA DC current for at least 10 days at 70ºC, corresponding to at least 3 months at 37ºC in PBS (assuming $Q_{10}$=2).

### PHASE 2 & 3: METALLIZATION REQUIREMENTS

Metallization for implantable applications has special needs compared to standard metallization in IC fabrication or packaging. The additional requirements are related with the final goal of the conductive material: it might be used as interconnect between various subcomponents of an active implant, or the material is used as a bio-electrode, hence it is realizing a direct electrical contact between tissue and the electronics. These requirements for materials to be used as in-vivo metallization are discussed in a previous publication [4].

In this paper we focus on the development of a biocompatible metallization scheme for the fabrication of interconnects between various chips (packaging phase 2) and between various sub-components of the final device (Phase 3). Excellent resistance against corrosion is important for such interconnects, since they are not covered with diffusion barrier layers. Due to the length of these metal patterns, very high conductivity is important to avoid high power consumption during device operation. Both gold (Au) and platinum (Pt) are excellent candidates for this application, with a small advantage for Pt due to its superior corrosion resistance. A drawback of both materials is that they are somewhat brittle, hence alloying them with another biocompatible metal (such as Iridium) or providing sufficient mechanical support is essential. In our packaging concept, the metal patterns will be embedded in polyimide, which thickness will have to be optimized in order to provide sufficient mechanical support. A second drawback of Pt and Au is

their cost. This topic is discussed extensively in the following section.

## COST EFFECTIVE FABRICATION OF PLATINUM METALLIZATION

For our packaging concept, we selected Pt over Au metallization due to its superior corrosion resistance, but Pt is even more expensive then Au. Since in each packaging phase of our packaging concept Pt metallization will be used, the cost of it will be important. Two Pt deposition processes are commonly used: sputtering combined with lift-off, and selective electroplating combined with seed layer deposition and later removal.

### *A. Cost of Ownership Calculation*

For both Pt deposition processes, a CoO calculation is performed and reported extensively in a previous publication [4]. In this paper only a summary is given below.

For Pt sputtering, recycling of Pt is a key factor for cost reduction. Pt targets have to be replaced before they are fully consumed, but target recycling is common and easy. Recycling of Pt scraping from walls etc. is possible but not straightforward, hence a cost efficiency of ~80% is realistic. Recycling of Pt from the lift-off fluid is far from standard due to the cost of handling and safety issues by the transport of the fluid, but recycling is not possible. The Pt sputter process with target recycling is further called 'S1', with additional scraping recycling is called 'S2', and with target, scraping and fluid recycling is called 'S3'.

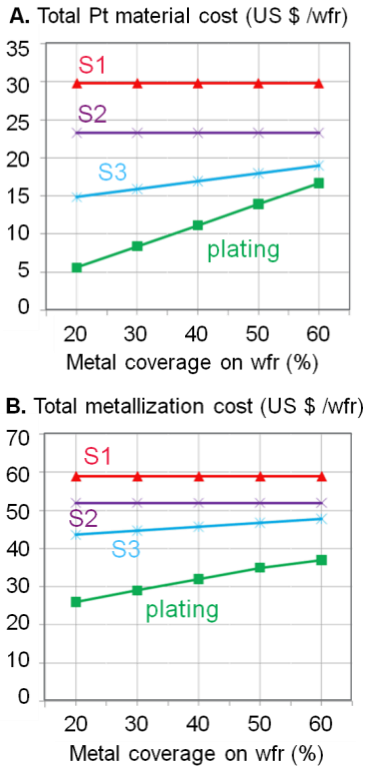


***Fig. 10:*** *(A) Cost of Pt material and (B) of the total Pt metallization step for one 200mm wafer, using Pt plating and sputter processes. S1, S2 and S3 are sputter processes with different recycling actions. Sputtering is always more expensive, even when maximum Pt recycling (S3) is applied.*

Fig. 10 shows the CoO calculations resulting in the Pt material cost and the total cost (tool, labor, material, etc) for one Pt metallization step on a 200mm wafer. Selective plating is obviously much more cost effective than sputtering, even when maximum Pt recycling is performed. For a Pt coverage of 30%, plating costs 30US$ a wafer, sputtering from 45 to 60US$, depending on Pt recycling options. For all cases, the cost of Pt metallization will form a considerable part of the total implantable package cost.

### *B. Development of a selective Pt plating process*

Based on the CoO calculations, we decided to develop a selective plating process for Pt, in order to have a cost effective metallization process for implantable devices. First a blanket plating process is optimized, later this process is adjusted towards a selective plating process. Details of this development are reported in Ref [10].

To start, a biocompatible seed layer needs to be selected for this electrochemical deposition of Pt. Tests with TiN and gold (Au) as seed layer are performed, nucleation and Pt growth studies have shown that best results are obtained using a PVD sputtered TiN seed layer. Two different electroplating solutions are tested: dihydrogen dinitrosulfatoplatinate (DNS) electrolyte and hexachloro platinic acid electrolyte. Pt films plated using DNS were smoother, hence this solution is selected for further work. Various plating parameters are evaluated, such as galvanostatic or potentiostatic plating control, current density/voltage settings, seed layer thickness and pre-treatments, bath pH, etc. All these parameters are optimized regarding Pt uniformity, adhesion, maximum thickness, stress, roughness of the obtained Pt film and deposition reproducibility. Smooth and relatively thick Pt films (up to 800nm) with good adhesion are obtained using a galvanostatic plating process on a 70nm thick TiN seed layer (Fig. 11).

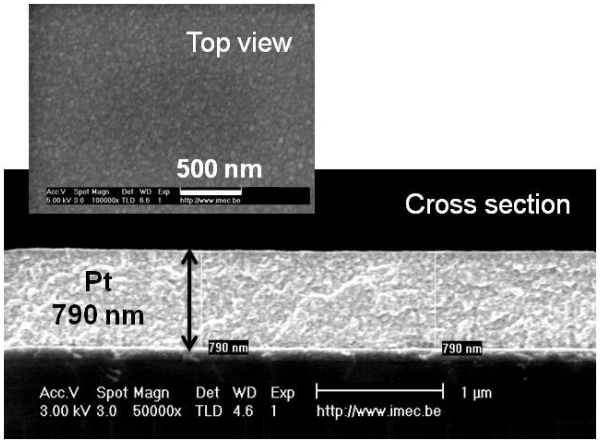


***Fig. 11:*** *Top view and cross section of the Pt film after plating optimization.*

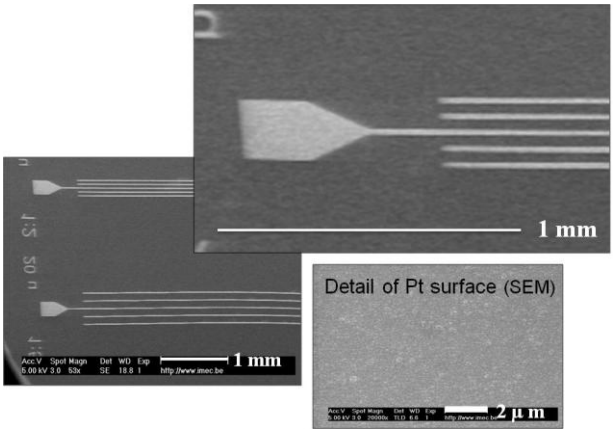


***Fig. 12:*** *~170nm thick patterned Pt interconnects show no pores or cracks. The patterns in the pictures are 20um wide, with varying spacing.*

Subsequently selective plating of Pt was performed on TiN/polyimide/glass substrates. Polyimide is selected as substrate since the chips will be packaged in polyimide in phase 2 of the packaging sequence. Both PI4110 and PI2611 polyimides from Hitachi-Dupont are used. The TiN is covered with a 3um thick resist pattern prior to plating. After the selective Pt plating step using the optimized process described above, the resist is stripped, leaving behind the desired Pt patterns on the polyimide film. The metallization process is finalized by removing the TiN seed layer in between the Pt patterns using an SF6 based plasma etch. Scanning electron microscopy (SEM) analysis revealed that ECD Pt lines were shaped uniformly with no pores or cracks and high pattern fidelity (Fig. 12)..

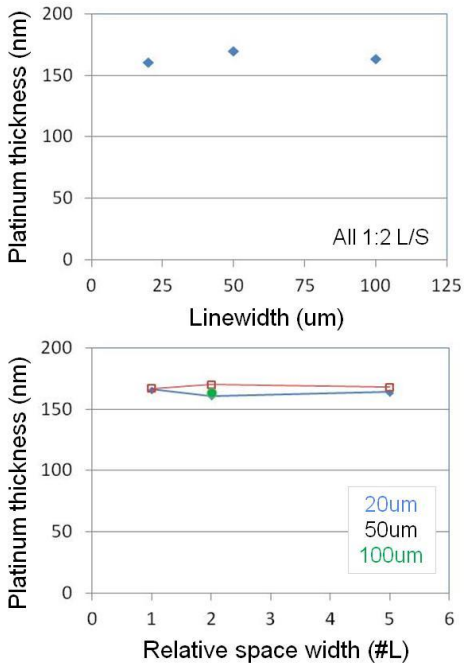


***Fig. 13:*** *Dektak Pt thickness measurements for various patterns show that the platinum thickness is ~165nm for all measured structures, independent of linewidth or spacing.*
*Top: comparison of thickness for various linewidth; bottom: for 20um and 50um lines, the Pt thickness is similar independent of spacing dimension.*

Lines with various width and spacing are patterned: linewidths are varying between 20um and 100um, spacing between 1 and 5 times the linewidth size. The thickness of the Pt patterns was measured using the Dektak surface profiler for various patterns. The results showed that the thickness of the Pt patterns was independent on the linewidth and on the spacing (see also Fig. 13), proving that a very good plating uniformity is obtained.

### *C. Resistivity of selective Pt film and patterns*

After fabrication of Pt patterns, the electric resistance of the Pt patterns was measured. For an interconnect length of 5.8mm, a resistivity of about 300Ω and 780Ω was found for 50um and 20um wide lines respectively. These measurements correspond to a resistivity of about 440 nΩ.m for the plated Pt film. Theoretically, a pure Pt film should have a resistance of 104 nΩ.m.

Based on these observations, it was decided to anneal the plated Pt film, in an attempt to reduce the resistivity by possible outgassing and/or crystallization. Annealing is typically performed for 3 hours under vacuum, but also shorter annealing times are used (10 and 150min). Annealing temperatures varied between 300 °C and 400°C. Resistance measurements before and after annealing are plotted in Fig. 14. Also for sputtered (PVD) Pt the resistance was measured and plotted. The beneficial influence of the annealing step is obvious. Higher annealing temperatures give slightly better results. The annealing time seems to be less important: even after annealing of only 10min a severe drop in resistivity is seen. It should be noted however that each

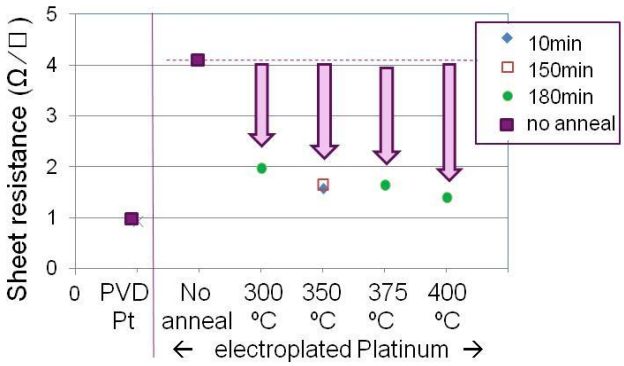


***Fig. 14:*** *Resistance measurements of Pt films before and after annealing,showing the succesful reduction of the resistance of plated Pt.*

annealing is done using a slow temperature ramp up and ramp down, hence even the 10min annealing time corresponds to a longer period annealing at temperatures close to the final annealing temperature.

When looking at blanket films before and aftr annealing, a clear change in color is observed, as shown in Fig. 15: before annealing, the Pt film is grey, after annealing the film is bright and reflective. FIB analysis showed that recrystallization occurs, which is reducing the resistance of the material.

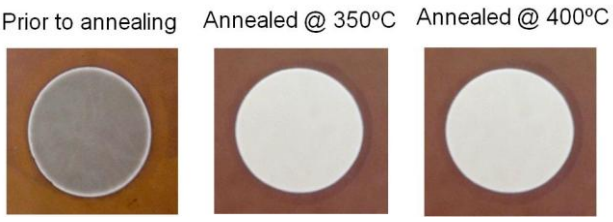


***Fig. 15:*** *Pictures of the Pt films before and after annealing. A clear color and reflectivity change is the result of recrystallization of the Pt film during annealing.*

Note that this annealing step don't has to be always an additional process step during the fabrication of the total package: the Pt pattern will be covered with a polyimide layer, which need a curing step of ~375°C during 2 hours anyway. This curing step is probably sufficient to reduce the Pt resistivity down to an acceptable level.

After fabrication of Pt patterns in polyimide, the polyimide was successfully released from the substrate. After release, the Pt metallization on polyimide forms a flexible interconnect pattern. The Pt pattern was sticking firmly on the polyimide film, also during bending of the polyimide. Tests to investigate the mechanical properties of the Pt film under static and dynamic bending are scheduled.

## CONCLUSIONS

A cost-effective, miniaturized and biocompatible packaging method for medical devices is proposed, resulting in a small, soft and comfortable implantable package.

Phase 1 of this packaging concept is largely explored; various common clean room materials are tested with respect to their suitability as biocompatible barrier layer. Cytotoxicity tests and Cu diffusion tests showed that several materials –both insulating and conductive materials- are interesting barrier layers. Regarding biostability, a SiC layer is found to be essential to protect less bio-stable SiNx, and a Pt layer is needed to protect conductive barriers in certain bio-environments. Both active and passive corrosion tests are performed proving that the Pt capped electrode structure is highly corrosion resistant.

Pt or Au are the most suited materials for the biocompatible metallization process required in phase 2 and 3 of the packaging sequence. CoO calculations showed that selective plating of Pt is less expensive than Pt sputtering, even with maximum Pt recycling. Hence an electrochemical plating process for Pt is developed for cost reduction of the final total packaging process. Plating parameters are optimized and a reproducible process is obtained enabling the deposition of a blanket 800nm thick Pt layer on a TiN seed layer. By selective plating using a resist pattern on top of TiN, Pt patterns down to 20um width are fabricated with good thickness uniformity. A simple annealing step between 300°C and 400°C has proven to be successful in reducing the plated Pt resistance, making the material suitable for the fabrication of long interconnects.

Although the implantable packaging process is not fully developed yet, important improvements are made and promising results are obtained.

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