Development of thin package using the glass carrier substrate

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Abstract

"The glass carrier substrate" formed on support glass using conventional build-up substrate technologies is developed. This substrate is ultrathin, and is suitable for the applications that thinner packages are highly demanded, such as for mobiles.

The advantage of glass as the carrier for the substrate is that the CTE of glass is close to that of silicon. The CTE matching of glass with silicon enables the narrow pitch mounting, because of reduced distortions between the chip and the substrate. When the chip is bonded on the substrate, glass is still combined with the substrate as the carrier. After chip bonding, the substrate can easily peeled off with laser irradiating through glass due to the characters of adhesive layer.

To verify the advantage, we prepared the thin substrate and made a connection with a narrow pitch (50um) bump chip, by means of Thermal Compression Bonding with non-conductive paste. The process of injection molding was used for packaging the substrate. We evaluated the reliability of the thin package, by temperature cycle test (JEDEC MSL-3+Cond.B). It was confirmed that the package passed the criteria.

It is convinced that the package with glass carrier substrate is an effective solution for making thinner packages.

Key words

glass carrier substrate, small distortion, small warpage,

I. Introduction

Recently, semiconductor packages particularly for mobile applications are strongly required to be thinner. [1][2] To meet these market needs, substrates need to be thinner as well. Semiconductor packages called Fan-out WLP are being provided to the market. The typical production method of the packages is chip first process: for example, semiconductor chips are fixed on the silicon supporting substrate. An insulating layer covering the periphery of a semiconductor chip is made, then releasing the supporting substrate. Re-distribution layer and external connection terminals to the semiconductor chip are made on the insulating layer. It seems to be general that silicon substrate and semiconductor production equipment are used for these applications. [3]-[7]

It is developed a thinner substrate named "the glass carrier substrate" which is fabricated on support glass using a conventional build-up substrate technology. Generally, normal build-up layers do not have enough mechanical strength, and it is impossible to form ultra-thin substrate consisting of only resin layer. However, glass carrier substrate technology is capable to form a very thin substrate. Even if package size becomes large, warpage of glass carrier substrate keeps in low level because of the stable stiffness of glass. The glass carrier substrate technology has the following advantages.

- Technology derived from conventional FC-BGA fabrication can be used.
- Conventional chip mounting technology can be used.
- Narrow pitch mounting with small distortion can be made.

The process is RDL first (Redistribution Layer-first). After chip mounting and molding, a support carrier is removed. An adhesive layer and the UV curable resin are used for removing a layer on one side of a transparent glass. After semiconductor chip is mounted then molded, laser light is irradiated from the surface of the other side of support glass to remove the glass carrier. Finally, a glass carrier substrate is produced.

The first step of the fabrication process of the substrate is to form an adhesive release layer and a copper foil on the top of the carrier glass. Wiring layers are made on the copper foil by using semi-additive and build-up method same as FC-BGA substrates.

After the whole wiring layers are completed, it is brought to assembly process. OSATs can mount the chip and mold with the assistance of the stable stiffness of the glass carrier. After the glass carrier and the adhesive layer are removed, the thin package is completed.

To verify the advantages, we made the prototype glass carrier substrate samples using glass panels. Furthermore, using the prepared glass carrier substrate, we made the ultra-thin package (350um) with 50um pitch peripheral chip.

In this paper, we describe the manufacturing processes of the glass carrier substrate and features of ultra-thin semiconductor package using the glass carrier substrate. Finally, we report the reliability test results and warpage of the ultra-thin semiconductor package.

II. Glass carrier substrate

Substrate Fabrication Process

The schematic process flow of the glass carrier substrate is shown in Figure 1. The soda glass with 1.1mm thickness was used as the glass carrier because CTE of glass (9ppm) is not influential on the final substrate properties and it is inexpensive. The first step was the deposition of the adhesive layer on the glass carrier, then the lamination of copper foil (5um) was followed. The adhesive layer was cured by UV (385nm) exposure through the glass.

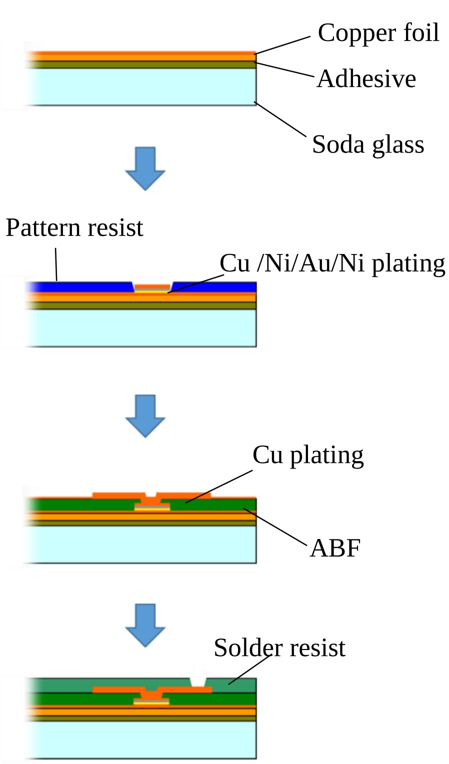


Fig.1: Schematic process flow of the glass carrier substrate

The wiring layer on the copper foil was made by semi additive process (SAP). Cu/Ni/Au/Ni plating in Fig1 becomes Cu/Ni/Au ball grid array (BGA) pad for connection with external connection terminals. Also, a resin film is laminated as an insulating layer. In this flow, ABF GX-T31R was laminated in vacuum as insulating layer, andφ50um via holes were formed with UV-YAG laser for interlayer connection. Via was formed by means of electrolytic copper plating. After solder resist forming, an OSP finish was provided on the copper conduction layer.

Since the conventional FC-BGA SAP process can be used for build-up layers with utilizing existing equipment, the manufacturing cost of this thin substrate can keep in low level.

Fabrication using 300mm□ Panel Glass

Compared to silicon processes, the manufacturing process using glass panel is easy to scale up, which helps to keep the process cost in low level. Also, compared to organic materials, the excellent smoothness of glass surface across the panel can support high yield for fine patterning.

In this paper, the glass carrier substrate fabricated using 300×300mm glass panel is described. The specifications are shown in Table 1 and the working panel appearance is shown in Figure 2. The adhesion between the glass carrier plate and the fabricated substrate was confirmed to be stable throughout the process without any delamination of adhesive layer. The build-up layers of the substrate were fabricated using TOPPAN's well proven FC-BGA technology. Neither defective appearance nor patterning failure caused from glass carrier process was found.

Through the process flow, the substrate which has two wiring layers with 70um of total thickness including solder resist (SR) was successfully obtained. A cross-section of the substrate is illustrated in Figure 3.

Table1: 300mm□ prototype specifications

Item	Content
Number of layers	3-layer（Wiring 2-layer＋BGA 1-layer）
Minimum wiring line width	L/S ＝10/10µm
Wiring thickness	9µm
Panel size	300×300mm
Package Size	17×17mm
Build-up layer thickness	70µm
Chip size	7.3×7.3×0.15mm

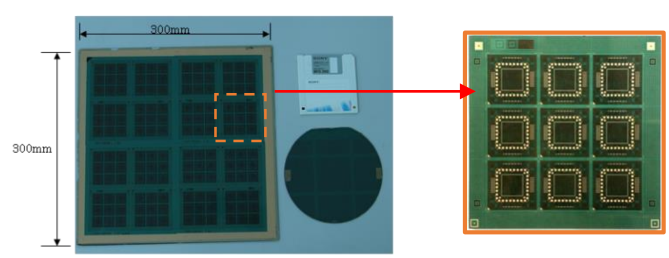


Fig.2: 300mm□ prototype appearance

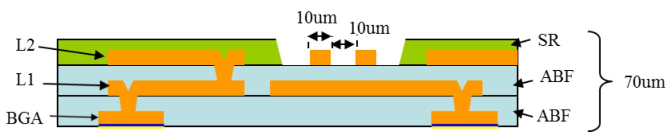


Fig.3: Cross-section of the build-up layers

III. Ultra-thin Package

Assembly Process

The semiconductor package was produced to examine the compatibility of the glass carrier substrate with assembly process. Figure 4 shows the process scheme.

The chip with 50um pitch peripheral connection was assembled by Thermal Compression Bonding method using Cu pillar bumps with lead-free SnAg caps on the glass carrier substrate (supported by SHINKAWA LTD). After chip attachment and mold resin encapsulation, the glass carrier was removed, by sublimating the de-bonding layer coated on the adhesive resin using Yb (1060nm) laser. The adhesive layer was mechanically peeled off by using a peeling tape. Then, the copper foil and Ni plate were etched out by wet process. Finally, the substrate was singulated with dicing equipment.

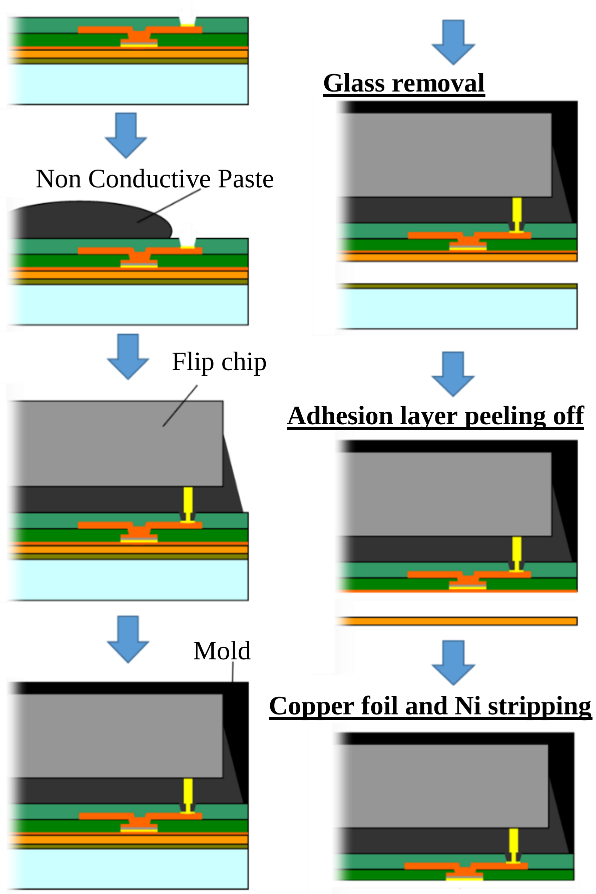
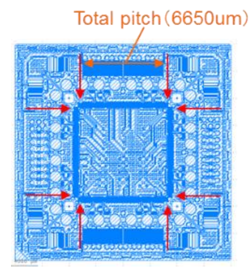


Fig.4: Schematic diagram of assembly process

Distortion Evaluation

In order to evaluate the glass carrier substrate distortion, a very thin substrate of 70um was fabricated on glass. The total pitch measurement result is shown in Table 2. As the total pitch design of 6650um, the measurement results and the design value is almost the same. The 3σ was very small within 3um.



[unit:um]

Item	Design	Average	3 σ
Total Pitch	6650	6650.3	2.7

Table 2: Dimension Measurement of the thin-substrate

The positional accuracy of the chip and the substrate was evaluated by X-ray observation. The relative position of the chip and the substrate is shown in Figure 5. It seems that the copper pillars were positioned exactly above the top of the peripheral terminals without any correction. This proved that total pitch is finished same as designed. The results showed that the distortion was small enough in the thin substrates and the size variation of the thin substrate was small, because distortion can be controlled by glass.

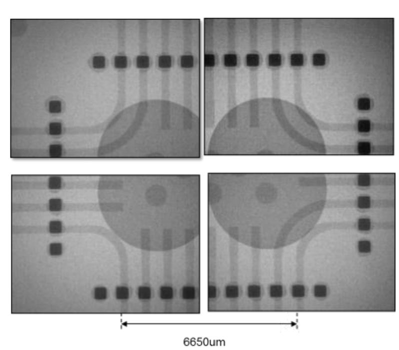


Fig.5: Alignment position confirmation of the chip and the substrate

Interconnection

The chip with 50um pitch peripheral connection was assembled by TCB method. Figure 7 shows the cross-sectional view of the package. It is usually difficult to attach the die onto normal build-up material without support, because it doesn't have enough mechanical strength. However, by using the glass carrier, die attachment becomes much easier even on the very thin substrate. It was proven that the connection between copper pillar of the chip and the substrate terminal was good, as described later in "Reliability".

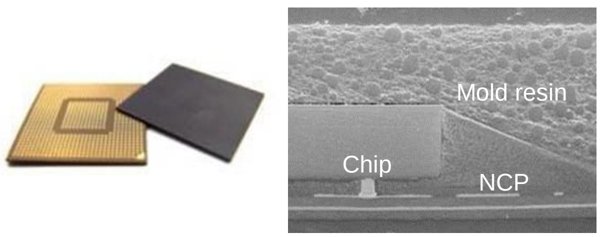
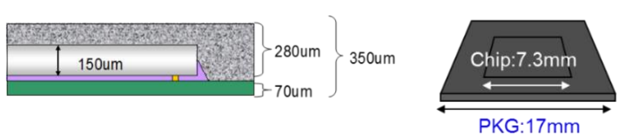


Fig.6: Cross-sectional view of the package using the glass carrier substrate

Package warpage

Figure 7 shows the warpage amount of the package (with mold resin, substrate and chip). This evaluation was done with mold resin supplied from Hitachi Chemical Co., Ltd. Mold resin contains epoxy resin and filler. The shrinkage rate of the resin was controlled by changing the composition of these elements. As a result, it was confirmed that the warpage changed with the shrinkage rate of the mold resin. It is considered that warpage can be controlled by using the appropriate mold resin even if the configuration of the build-up layer changes.



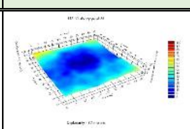
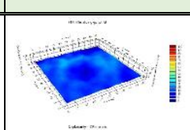
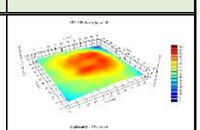
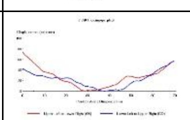
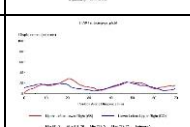
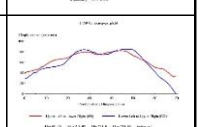
Mold resin	A	B	C
Shrinkage rate (%)	0.16	0.1	0.06
3D			
diagonal			
wapage	+73um	-29um	-83um

Fig.7: Warpage of molded packages (with substrate and chip) using mold resin with the controlled shrinkage rate.

Reliability

We evaluated the reliability of the thin package. We measured electrical conduction by means of temperature cycle test (JEDEC Pre-con MSL-3 + Cond.B -55℃～125℃), to check the connection between the chip and the substrate and the wiring inside of the substrate. There were two nets of daisy chain within a single chip. The nets were designed for evaluating connection between the chip and the substrate (inside the red line) and in the substrate such as via (outside the red line). Figure 8 shows the results of the temperature cycle test. Before and after the reliability testing, none of remarkable change was found in appearance, color, delamination, voids among layers and crack in via, from visual and cross-sectional inspections.

Test condition: Pre-con MSL-3 + Condition B(-55℃～125℃)

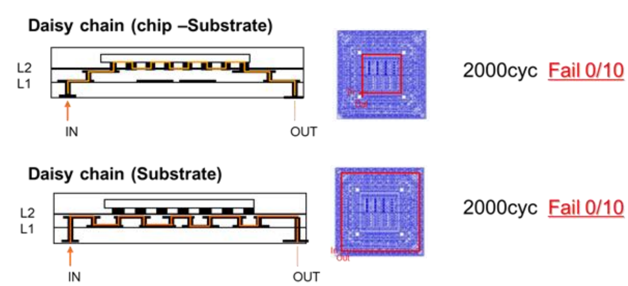


Fig.8: Reliability test results

Ⅳ. Conclusion

"The glass carrier substrate" is fabricated on copper foil laminated glass using conventional build-up technologies. Because of using glass as support, the distortion and warpage are small. This is compatible with conventional bonding machines so that semiconductor chips are mounted with conventional bonding processes. After molding, the carrier glass is removed, and the thin package is completed. Prototype samples were successfully obtained. Total pitch measurement results and the design value is almost the same (6650um), 3σ is also small. It was found that distortion can be suppressed by using the glass.

The matching of CTE between glass and silicon makes the narrow pitch mounting easier, because of reduced distortions between the chip and the substrate. To verify these advantages, we prepared thin package (350umt) with glass carrier substrate and made a connection by using a narrow pitch Thermal Compression Bonding (50um pitch). The observation of the joint point showed the positional accuracy between the chip and the ultra-thin substrates was in the allowance. The thin substrates (70um) were obtained and evaluated in this work. More investigation to find suitable materials can make thinner substrates and thinner packages feasible.

In addition, we evaluated the reliability of the thin package, by temperature cycle test (JEDEC Cond.B with Pre-con MSL-3) and confirmed the package passed the criteria. There was no defect within the 2000 cycles.

In conclusion, the glass carrier substrate has excellent features,

- Distortion was small
- Warpage was small (29um) in 17mm square package size
- The ultra-thin substrate (70um) and package (350um) could be made

Additionally, it is possible to reduce cost for production by applying conventional equipment and using a large panel,.

We convince that "the glass carrier substrate" is an effective solution for making thinner packages.

Acknowledgment

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