APPLICATIONS OF SOLDER PREFORMS TO IMPROVE RELIABILITY

Carol Gowans, Seth Homer
Indium Corporation, Utica, NY

Ronald Lasky, PhD, PE
Indium Corporation, Dartmouth College, Woodstock, VT

ABSTRACT

As early as the 1990s people were predicting the end of through-hole components, but they are alive and well with the numbers of dual in-line packages (DIPs) and connectors still measured in the 10s of billions per year. Many of these components are assembled by wave soldering, however in mixed technology (SMT and through-hole on the same board) where the through-hole count is low, it is often advantageous to consider selective soldering or the pin-in-paste process (PIP). PIP is a process in which solder paste is printed over or near the PWB through-holes. The through-hole components are then placed and the solder joint is formed during the reflow process. PIP has the advantage of eliminating the wave soldering process step. In many cases it is difficult to print enough solder paste to make an acceptable through-hole solder joint. Solder preforms were developed to meet this need.

These solder preforms are typically shaped in the form of 0402, 0603, or 0805 passive components. The preforms are placed on the appropriate printed solder paste deposit by a component placement machine. Preforms come in tape & reel packaging.

Today solder preforms are also used in other "solder starved" applications such as radio frequency (RF) shields, connectors, and under QFN thermal pads. In all cases, the extra solder delivered by the preform is vital to the reliability of the assembled product.

In this paper, process, design, and assembly methods for solder fortification using preforms will be discussed. Four successful solder fortification examples will be presented along with the associated defect reductions.

Keywords: Solder preforms, pin-in-paste, solder fortification, solder starvation, mobile phone shields, QFN packages, flux

SOLDER PREFORMS

Solder preforms used in SMT assembly will typically be in the shape and approximate thickness of 0201, 0402, 0603, or 0805 passive components. The preforms will usually be packaged in tape & reel. See Figure 1. In most SMT processes using preforms, the preforms will be placed by a component placement machine in the same manner as the components. Hence, the solder paste will be printed first then the preform placed. The preforms can be made of any solder (e.g. lead-containing or lead-free) and can be flux-coated or free of flux, depending on the application.

Figure 1. Solder preforms for SMT applications are typically 0201, 0402, 0603, or 0805 in shape and are packaged in tape & reel.

APPLICATION I: MINIMIZING VOIDING IN QFN GROUND PLANE SOLDERING

The QFN (quad flat-pack no leads) is the most commonly assembled integrated circuit package after the SOIC (small outline integrated circuit.) About 30 billion QFNs will be placed in 2012, almost 15% of all packages assembled.

Unfortunately, QFNs are susceptible to voiding between their ground plane and the PWB pad when assembled with solder paste. This voiding occurs due to the excessive flux in the solder paste and the lack of standoff of the component. Using a solder preform can minimize such voiding by adding solder volume to the joint without adding significant flux.

The QFN package has no leads and has a thermal pad that must be bonded to a receiving pad on the PWB. See Figure 2. The QFN assembly process is essentially a standard SMT process. Solder paste is printed on the PWB lead pads as well as the PWB thermal receiving pad.

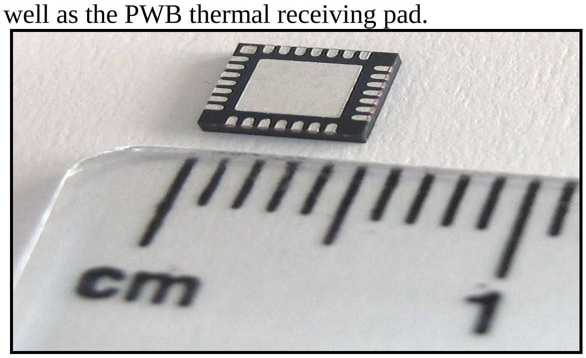

Figure 2. A QFN showing its leads and thermal pad pad for the QFN thermal pad.

Then the QFN component is placed by the component placement equipment. The QFN design leaves little vertical space between the QFN thermal pad and the PWB pad. Therefore, during the reflow process, some of the flux volatiles do not escape, but end up forming voids in the thermal pad area.

The level of voiding that is acceptable will vary depending on the component and the application. However, the most common QFN concern relates to the largest void created between the thermal pad and the PWB pad. Solder preforms, in conjunction with the paste deposit, will reduce the size of the large voids and as reduce the overall quantity of voids.

Figure 3 shows such voiding. Some QFN designs are large and require more solder paste than printing can achieve. In such cases, the lack of solder is responsible for the voiding. The voiding is more than a cosmetic concern as poor thermal conductivity between the QFN pad and the PWB can result. This lack of thermal conductivity can lead to IC reliability concerns.

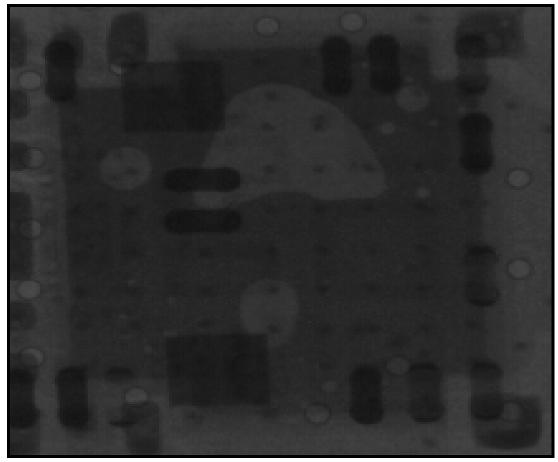

Figure 3. An X-ray image of the voiding between the QFN thermal pad and the PWB

Developing a the Process

Developing a successful process to minimize voiding requires attention to the stencil design, the preform geometry, the preform placement parameters, the preform flux coating, and the reflow oven profile.

Stencil Design

When using a solder preform, the stencil design parameters vary, but experience indicates that stencil designs that maximize the solder paste under the component result in less voiding. A good starting point is following the QFN manufacturer's design recommendations. See Table 1.

Freescale Semiconductor AN1902
Application Note Rev. 4.0, 9/2008

QFN	PCB Land Pattern				Stencil Aperture			
	4 x 4		9 x 9			4 x 4		9 x 9
Version	E	S	E	S	E	S	E	S
Lead pad width (mm)	0.37	0.37	0.28	0.28	0.32	0.32	0.28	0.28
Lead pad length (mm)	0.92	0.92	0.69	0.69	0.75	0.75	0.69	0.69
Pitch (mm)	0.65	0.65	0.50	0.50	0.65	0.65	0.50	0.50
Thermal pad width (mm)	2.15	2.15	7.25	7.25	2.15	2.15	7.25	7.25
Thermal pad length (mm)	2.15	2.15	7.25	7.25	2.15	2.15	7.25	7.25
Aspect ratio	—	—	—	—	2.52	2.52	2.20	2.20
Area ratio	—	—	—	—	0.88	0.88	0.78	0.78

Table 1. An example of stencil calculation based on the Freescale QFN Application Note AN1902

Preform Geometry

Experiments we have conducted show that minimum voiding occurs when the preform occupies about 80 to 85% of the PWB thermal pad area. The preform thickness should be about 50% of the thickness of the solder paste deposit, but must be at least 0.0015 inches (0.04 mm) thick to avoid unacceptable bending of the preform. See Table 2.

Preform Design:

QFN	
4 x 4	9 x 9
Thermal Pad	
2.15 x 2.15	7.25 x 7.25
Preform Geometry	
1.83 x 1.83	7.25 x 7.25
.002"	.002"

Table 2 The calculation for suggested solder perform dimensions.

The metrics in Table 2 are suggested starting points; each individual process may require some optimization. As an example, a larger pad area might require a solder perform closer to 80% of the pad area. As the solder paste must provide tack for both the preform and the QFN, designing the stencil to allow for paste around the perimeter of the preform will enable the paste to secure the QFN and the preform.

Placement Recommendations

Figure 4. A rectangular solder preform placed on the solder paste.

The preform must be placed with enough force so that it is pushed into the paste far enough so that the QFN makes contact with the solder paste. See Figure 4. If this is not done, the QFN will float and not be properly soldered. The placement force for the QFN must also be great enough to assure that it is seated well into the paste so that a good solder joint is possible.

The increased placement pressure on the preform can result in bending. To minimize preform bending the component placement nozzle should be as large as possible, as shown in Figure 5.

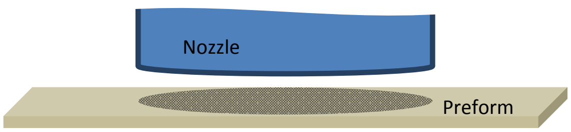

Figure 5. The component placement nozzle should be as large as possible to minimize preform bending.

Flux Coating

The interface between the top of the preform and the thermal pad on the QFN has no solder paste and hence no flux. This situation could make voiding worse. In light of this need, preforms are typically coated with 1 to 1.5% by weight NC-9 flux as shown in Figure 6.

It is important that the flux coating be compatible with the solder paste used.

Figure 6. To minimize voiding the solder preform must be flux-coated as shown

Reflow Profile

The addition of a preform does not require adjustments in the SMT profile used.

Results

Studies have shown that by using solder preforms in QFN assemblies, the resulting voiding average was less than 10%, with a 50% reduction from initial voiding levels.

APPLICATION II: THE PIN-IN-PASTE PROCESS [i]

The mechanical strength of through-hole connections is critical for applications such as connectors. A personal computer is a prime example with multiple USB, and power and video connectors that must withstand multiple plug-ins. However, these connectors are still relatively few in number, making the wave soldering process expensive, as well as a possible yield and reliability risk. In these cases, an alternative to wave soldering may be selective soldering or perhaps the pin-in-paste (PIP) process.

In the PIP process, a calculated amount of solder paste is printed over or near the through-hole. The through-hole component is placed and sent through the reflow process along with the SMT components. Hence, it is important to verify that the through-hole component can withstand the SMT reflow temperatures. The development of an effective PIP process is reviewed in references 1 and 2.[ii,iii] PIP is typically performed with no-clean solder paste.

Solder paste is about 50% by volume flux. This fact, and because so much solder paste is used in the PIP process, residual flux is a concern. This residual flux can make in-circuit testing difficult. Figure 7 shows excess flux on through-hole pins after the PIP process.

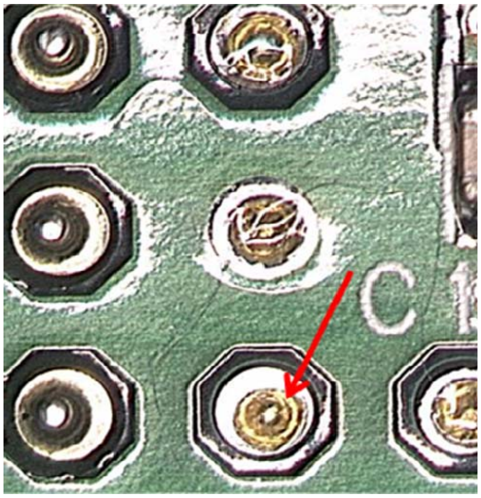

Figure 7. The arrow points to a pin soldered with the PIP process. Note the excess flux.

Solder starvation is also a concern in the PIP process. See Figure 8. The reason for this lack of solder is that it is often difficult to print enough solder paste to form a good

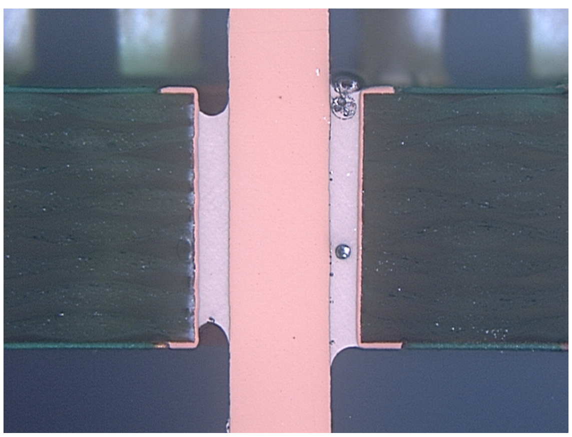

Figure 8. Note the lack of solder in this PIP through-hole solder joint.

through-hole solder joint. The solder joint in Figure 8 may pass ANSI/J-STD-001C, but most process engineers would not find such solder joints acceptable from a quality/reliability perspective.

Using solder preforms in the PIP process will minimize these types of problems. As stated earlier, PIP solder preforms are rectangular in shape and are of the size of common passive components (e.g. 0201, 0402, 0603, etc) facilitating their placement by component placement machines.

The PIP solder preform process uses current equipment and SMT process parameters. A typical PIP with preforms process follows:

1) Solder paste is printed on the pad of the through-hole pin. The precise volume of solder paste can be calculated with free Excel® software such as StencilCoach™ [iv]. See Figure 9. The solder paste printed in this fashion will enable the solder to wick to the pin.
2) Preforms are then placed in the solder paste with component placement machines. See Figure 10.

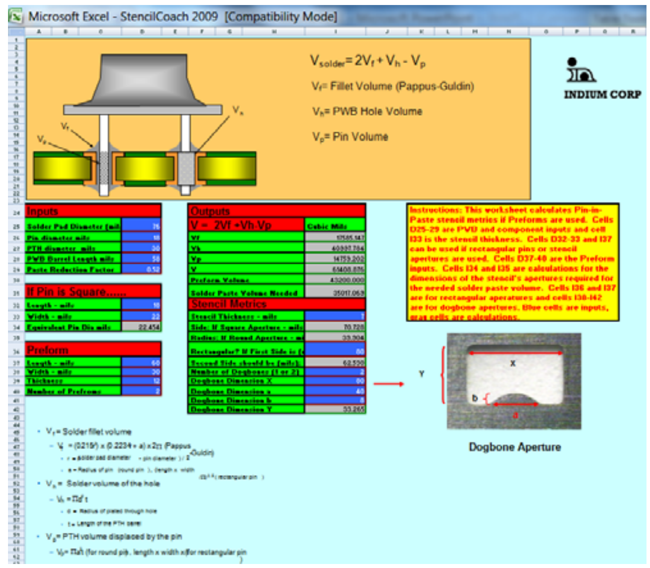

Figure 9. StencilCoach™ can make stencil and preform calculations easy.

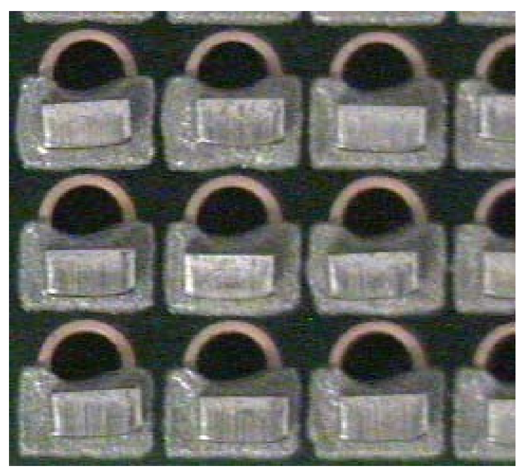

Figure 10. Solder paste is printed and the preforms are placed on the paste as shown.

The PIP plus preforms process not only produced the excellent results seen in Figure 11, but since there was no excess flux residue, the quality of the joint is easy to visually access and there was no loss of assembly line throughput.

This process not only enables an SMT only process with no additional process steps, but the quality and reliability of the solder joints are excellent.

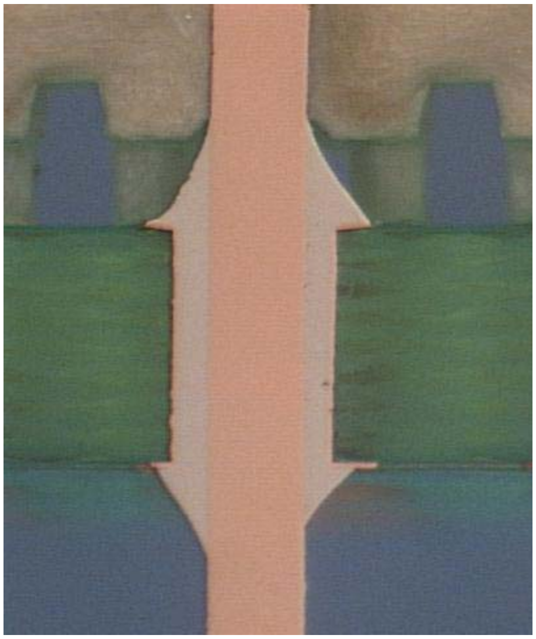

Figure 11. The solder preform + solder paste solution delivered excellent through-hole solder joints.

APPLICATION III: GROUNDING OF MOBILE PHONE SHIELDS [i]

Mobile phones are actually radios. As such they are susceptible to interference from stray electromagnetic (EM) radiation and electrostatic discharge. To minimize the deleterious effects of these phenomena on mobile phone performance, Faraday shields are often mounted over critical circuitry. Figure 12 shows Faraday shields over most of the integrated circuits on a mobile phone PWB. These shields are assembled along with the other SMT components. To assemble the shields, solder paste is printed on the receiving pads on the PWB and the shield is then placed with component equipment onto the solder paste. The shields are then soldered, with the other components, in the reflow process.

Many of the new, highly dense, mobile phone designs are such that it is often difficult to print enough solder paste to form an effective solder joint to connect the shield electrically to the PWB pad. In such cases the shield will not perform its EM and ESD protection tasks.

Solder preforms are often used in such solder starved conditions. The preforms are placed by a component placement machine as shown in Figure 13.

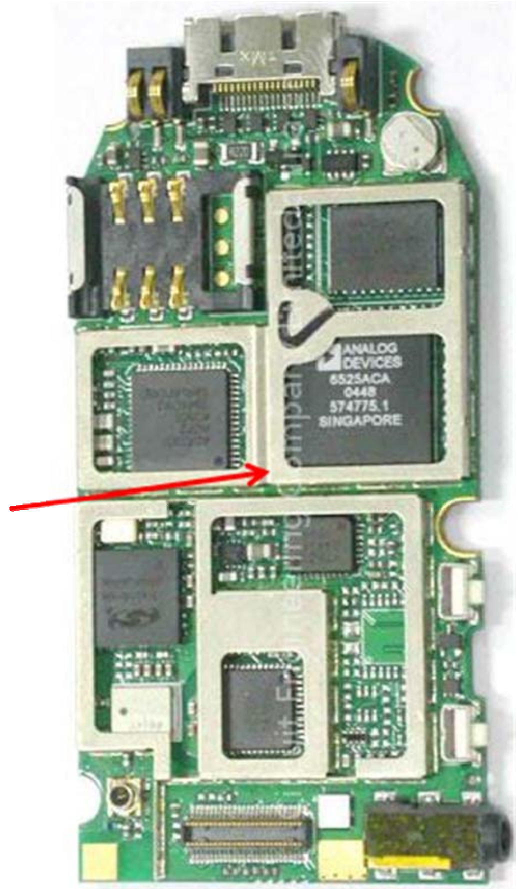

Figure 12. A mobile phone PCB showing a Faraday shield. Many shields are not cut away as these are. Photo courtesy of China Telecon.

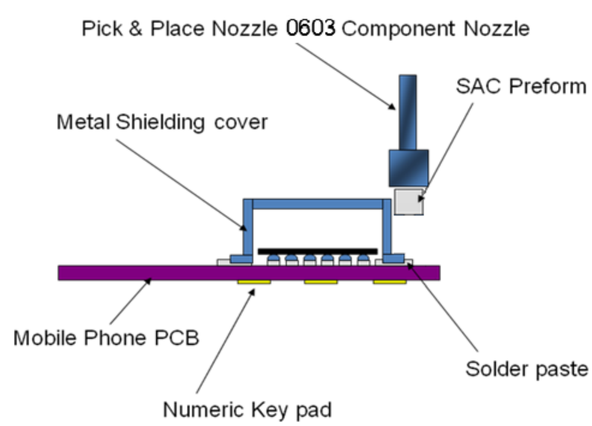

Figure 13. The SAC preform is placed by the component placement machine in the location.

In most cases a SAC (tin-silver-copper) preform is used and is the size of an 0603 passive component. See Figure 14. However, it is advisable to perform calculations to assure the preform used will deliver the correct amount of solder.

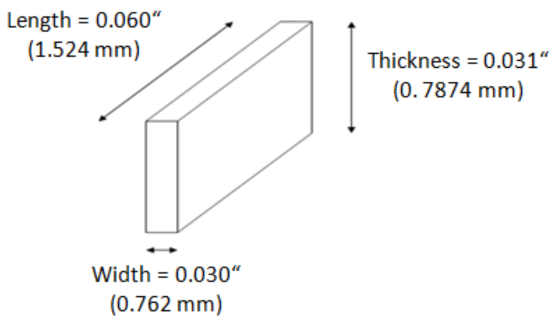

Figure 14. The 0603 preform used in the application as discussed in the text.

The preforms cost about $0.027 (US) apiece in quantities of 25 million. The application of this preform resulted in significant cost savings and increases in reliability.

Capacitor terminals can also experience solder starvation. In one such application, 0603 size preforms were placed near the capacitor terminals. In this application, the number of solder starved related defects was reduced by 95% after using preforms.

OVERALL CONCLUSIONS:

Solder preforms can dramatically increase solder hole-fill and the quality of the solder fillet in the pin-in-paste process. These improvements can result in overall improvement in the quality and reliability of the products assembled with the PIP process.

Preforms can also aid in other solder starved processes such as mobile phone Faraday shield and capacitor assembly.

However, with the proliferation of QFN packages, perhaps solder preforms most important role in SMT assembly will be aiding in the minimization of solder voids in the assembly of this important component package.

REFERENCES

[i] Although rewritten, parts of these sections were presented in *Solder Fortification with Preforms*, by Gowans, C. and Lasky, R. C., SMTAI, Orlando, FL, 2010.

[ii] Lasky, R. C., Jensen, T., *Practical Tips in Implementing the "Pin in Paste" Process*, at SMTAI, Chicago, IL, Sept 2002.

[iii] Berntson, R. B., Lasky, R. C., Pfluke, K. P., *Through-Hole Assembly Options for Mixed Technology Boards*, SMT Magazine, August 2004

[iv] StencilCoach™ can be obtained free from Indium Corporation: rlasky@indium.com.