High Temperature Packaging for SiC Power Transistors

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Abstract

Power transistors based on silicon carbide (SiC) are now commercially available. They have a higher efficiency and higher voltage blocking capabilities than conventional silicon devices. The wide-band gap and chemical inertness of SiC makes it suitable to high temperature operation. However, there is a need for new packaging for power transistors that can operate in higher temperatures. We have developed a package based on ceramics and silver for high temperature operation of SiC power transistors. Three types of SiC devices from different manufacturers are packaged and tested in room temperature. Though the devices were still functional after the packaging process, their performance seem to have degraded. This could be a result of the high temperature packaging process and the measurement setup. FEM simulations are also performed to investigate the thermo-mechanical behavior of the package. The target operating temperature of the package is 400 °C. Modeling show stress concentrations at the corners of the device chip and suggests that this stress is decreased if the substrate metallization is changed from copper to silver.

Key Words: SiC, packaging, BJT, MOSFET, high temperature

INTRODUCTION

In addition to increasing performance in applications where traditional Si-based components operate today, SiC-based power components are expected to be introduced into new applications where the operating environment exceed the limitations of Si systems. This could include for example oil well equipment, distributed drive systems in the automotive field or power stages for space exploration probes or landers, where ambient temperatures can reach above 400 °C. [1] demonstrated operation of a Shottky-barrier FET transistor at temperatures up to 400 °C. Other work includes [2] in which a SiC MESFET packaged in ceramics were demonstrated to 500 °C.

However, expansion into these applications requires that the packaging also is adapted for the high temperature environments. Since the peak temperature limit for electronics packaging generally is around 200-250 °C and in most cases lower for long term reliability, packaging based on new materials and processes are required.

SiC diodes have been available for several years from the Cree and Infineon corporations. In 2008 the SemiSouth corporation released a SiC JFET and in 2011 a SiC MOSFET was released by Cree. A SiC BJT is planned to be commercially available from Fairchild Semiconductors later this year. The packaging for these devices are based on traditional Si packaging which generally have maximum temperatures in the range 200-225 °C (The BJT used here will be

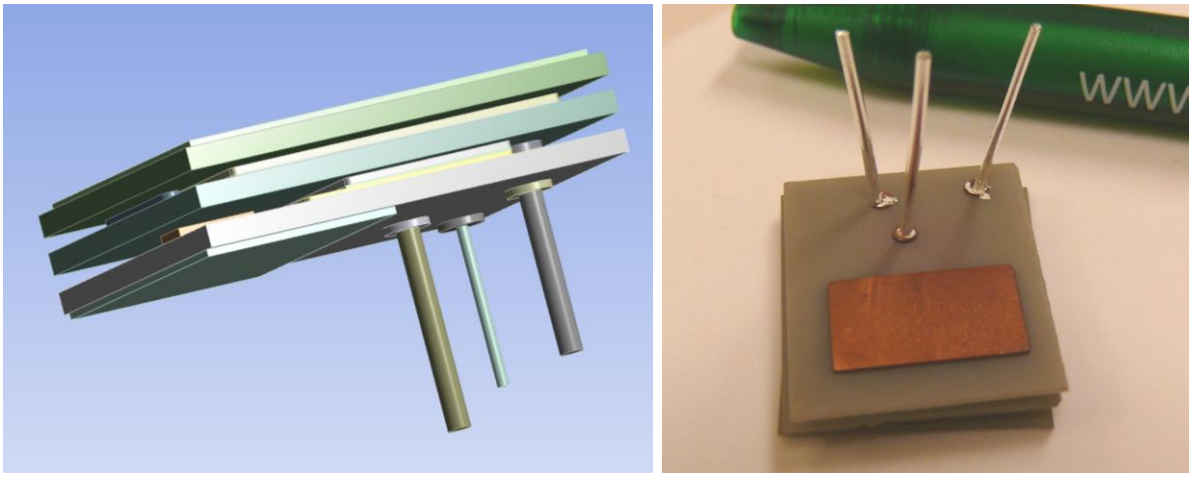

Figure 1: CAD image and photograph of the first sandwiched package. Coolers can be attached to top and bottom metallization facilitating double sided cooling directly above and below the device position.

available in a TO-258 package and have a specified maximum temperature of 250 °C). This is still much below the theoretical limit of operation for a SiC device. Several groups have started to investigate novel packaging alternatives for these and other devices [3, 4, 5, 6] that can extend the operational temperature and increase the reliability of SiC devices at high temperatures.

Here, we introduce a package design based on ceramic substrates and silver die attach in a sandwich arrangement. The package is designed to allow for double sided cooling. Packages based on DBC (direct bonded Cu) substrates with two types of SiC MOSFET devices (On-state resistance specified as RDS_{ON} = 80 and 160 mΩ) BJT devices have been manufactured and their functions are verified. In addition, a novel method of producing ceramic substrates coated with silver is introduced.

PACKAGE DESIGN AND FABRICATION

The design of the package (Figure 1) is based on 3 ceramic substrates with patterned conductors on both sides in a sandwich arrangement. An active SiC power electronics chip is embedded inside the sandwich structure. Electrical connections to the chip top side (usually the gate/base and source/emitter connections for FETs/BJTs) are made using filled vias through one of the ceramic layers. The electrical connection to the backside of the chip (usually drain/collector for FETs/BJTs) is made using nano silver die attach. The package design allows for several mounting geometries. The pins protruding from the bottom of the stack can be bent 90 degrees so that the stack of substrates can be mounted standing up. The design allows for cooling to be directly attached to conductive pads on both sides of the package directly above and below the active device using a thermal interface material (TIM).

The electrical connections on the chip is connected through buried vias to different conductive-layers in the stack. The layers are then accessed with pins inserted into a different set of vias to externally connect different layers.

The holes for the vias are made using abrasive water jet technology. This technology have previously demonstrated 0.4 mm diameter holes through ceramic materials [7]. The minimum diameter required is for the gate via of the BJT package, which is

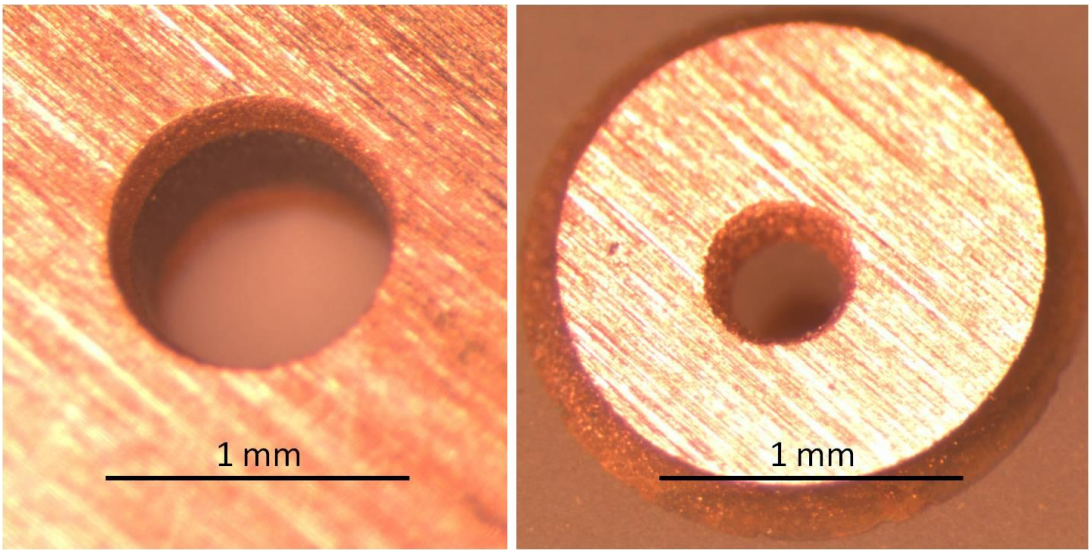

Figure 2: Holes of 0.98 mm (left) and 0.42 mm (right) diameters through the AlN DBC substrate made using abrasive water jet technology.

0.4 mm. The other vias are 1 mm diameter. Figure 2 show microscope images of holes made with abrasive water jet technology through the DBC substrates. The speed of the machining is set by the feed rate of the abrasive. Normal machining speeds are 9-27 mm/s for ceramic materials and the feed rate effectively sets the accuracy of the hole diameter. Faster cutting produces more accurate results. However to avoid delamination of the front or back Cu-layer it was found that the feed rate needed to be extremely low. This effectively reduced the speed of cutting by more than 90 % compared to cutting bulk ceramic materials. As a result the accuracy in the diameter of the holes is reduced and a rounding of the Cu edge occurs.

The design allows for different materials to be used. Here, DBC (direct bonded Cu) substrates are used, which are made up of a central AlN substrate (600 um thick), oxidized to form a thin Al_2O_3 layer at the surfaces and then eutectically bonded to Cu foils (300 um thick) on each side. The Cu were then patterned and etched to form the metalized traces and pads in the design. The final step before assembling the sandwich is to make the holes in each substrate layer separately using abrasive water jet.

Since both the BJT and MOSFET devices are delivered with Al contact pads an oxidation protective Ni/Au layer needs to be grown on the pads using an electro-less plating process.

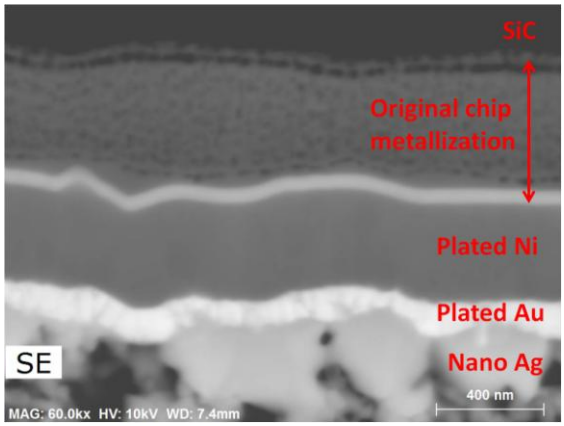

Figure 3: SEM image of the resulting layers on the collector pad of a SiC BJT after zincate treatment and Ni/Au plating.

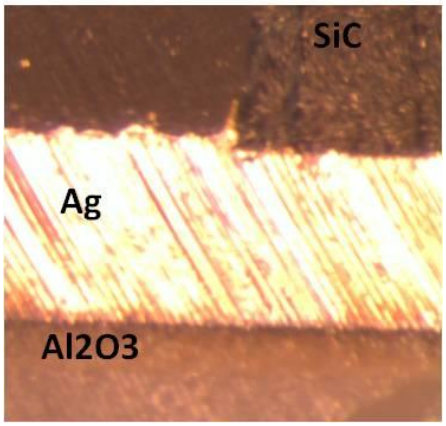

Figure 4: Cross-section of a Al_2O_3 substrate with silver foil and a SiC BJT.

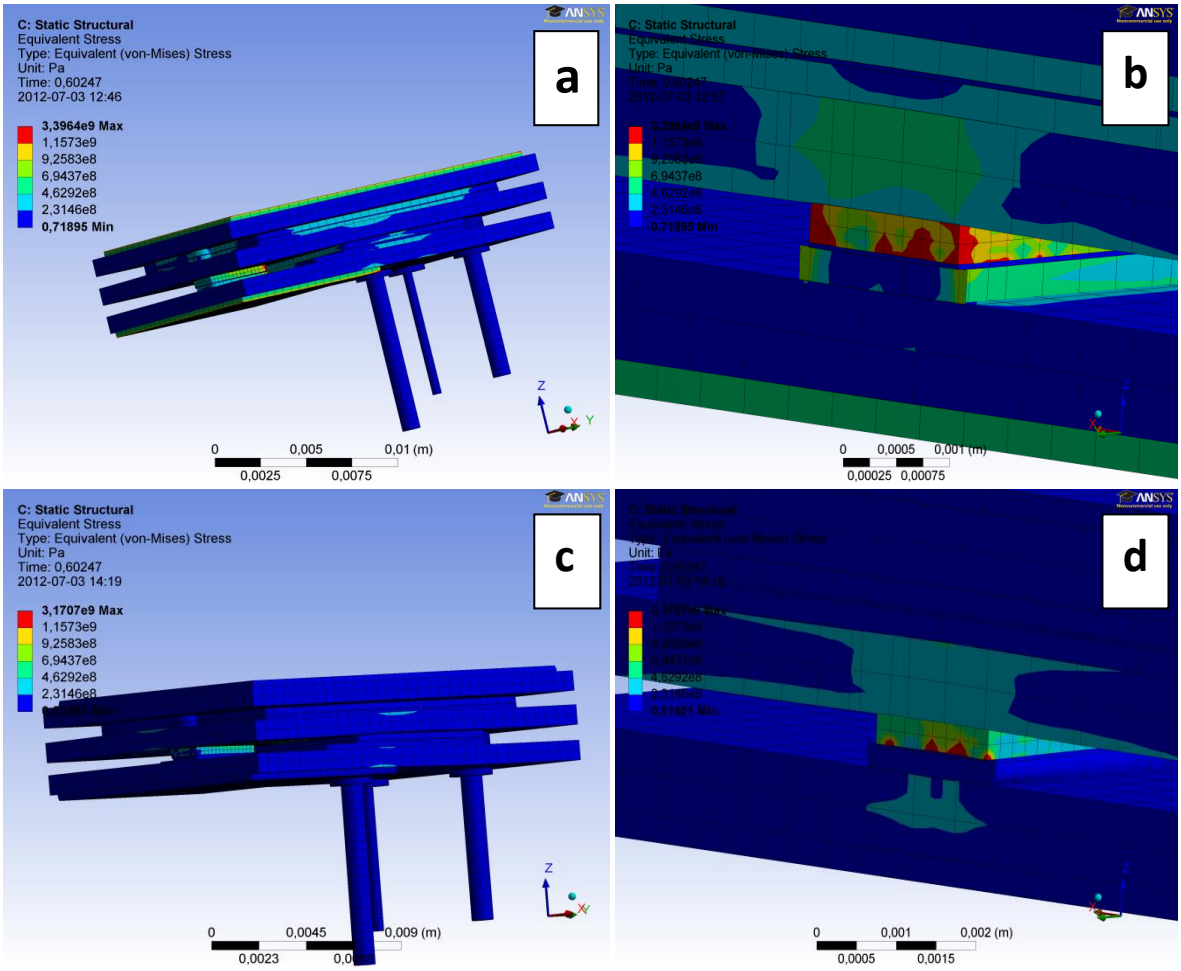

Figure **5: Equivalent stress in a packages using AlN/Cu/Ag (a, b) and Al2O3/Ag/Ag (c, d) substrates.**

The plating process involves an initial etching step with HNO_3, then a zincate treatment before plating in a Ni-solution for 20 minutes to for a 2 - 3 µm thick Ni layer. The Ni surface is then Au plated in an immersion Au solution. Figure 3 shows a SEM image of the resulting layers on the collector pad of a SiC BJT.

Before applying the die attach between the layers the surfaces are mildly polished to remove surface oxides and remnants of abrasive materials from the surfaces. The bottom two sandwich layers are then assembled using a nano-silver die attach supplied by NBE Tech, Virginia [8]. The nano-silver is sintered for 1 hour at 350 °C. The sintering is performed in a nitrogen atmosphere to prevent oxidation of the Cu surfaces. The assembly is allowed to self-cool inside the furnace. Typical cooling time to 70 °C is 3 hours. The top layer and the pins are assembled in a second sintering run. After the sintering process the devices have been exposed to temperatures above 200 °C for more than 4 hours.

As an alternative to the DBC substrates a material combination consisting exclusively of a ceramic and Ag is considered. The dielectric substrate material is then alumina (Al_2O_3) or aluminum nitride (AlN) and the Ag can be deposited via sputtering, screen printing or ink-jet printing, using a Ti adhesion layer or an Ag-paste or ink with a glass constituent to promote adhesion to the ceramic. An Ag foil of desired thickness suitable for the electronic application can then be attached to the thin

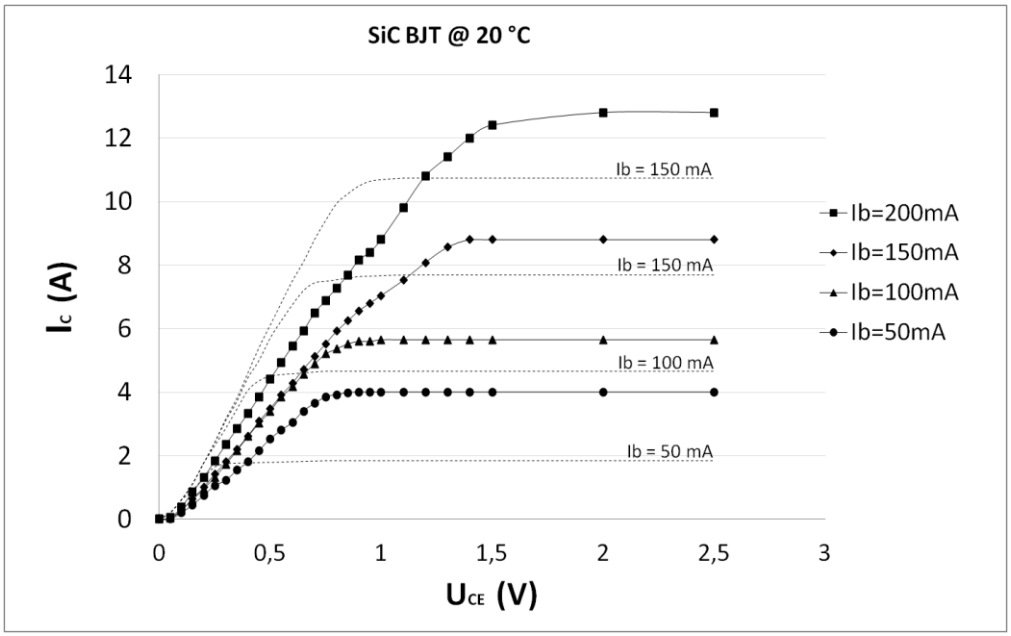

Figure 6: I-V characteristics of a packaged SiC BJT. The dotted lines are I-V data from the manufacturer.

Ag layer on the ceramic using for example nano-silver sintering. The thickness of the Ag could also be increased with electroplating to the desired thickness based on the power requirements of the electronics. The processes to make the substrate patterning and vias using ink-jet are described in [9]. Figure 4 shows an cross-section image of a Al_2O_3 substrate with a sputtered Ti/Ag, then a 300 µm thick Ag foil to which a SiC BJT have been attached using nano-silver. The thermal expansion of the Al_2O_3 is The final step in the packaging process involves sealing everything with a glass that matches the ceramic in thermal expansion. This step serves to insulate the device electrically and to prevent migration of the Ag in the presence of oxygen at high currents.

PACKAGE MODELING AND TESTS

Thermo-mechanical modeling have been performed to find stresses and strains within the designed package. ANSYS was used in the evaluation. The surfaces of the top and bottom conductive areas used for cooling attachments were constrained from movement and an ambient temperature of 400 °C was applied to every visible surface of the design. Self heating of the junction during operation is ignored.

The modeled geometry was simulated with both the AlN/Cu substrates and the Al_2O_3/Ag substrates. It should be noted that for a number of reasons (mostly lack of material property data for the simulated temperatures) the accuracy of these simulations is low. However, though there are errors in the absolute values the simulations should still be able to predict problematic areas with high mechanical stress and strain.

The results of the simulation of the AlN/Cu model (Figure 5) show low levels of equivalent stress in general except on the corners of the chip where several orders of magnitude higher levels are detected. In the Al_2O_3/Ag model the stress is reduced in these areas possibly due to the lower Young's Modulus of Ag (E_{Ag} = 35 GPa compared to E_{Cu} = 117 GPa).

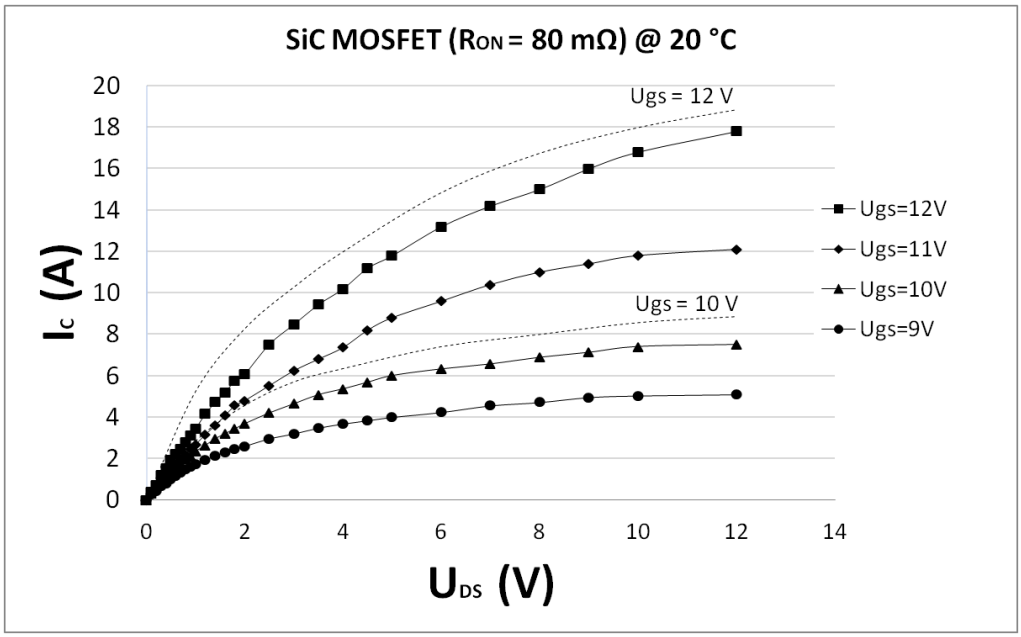

Figure 7: I-V characteristics for a packaged SiC MOSFET (specified as Rdson = 80 mΩ). Data from the manufacturer for Ugs = 10 V and Ugs = 12 V are plotted as dotted lines.

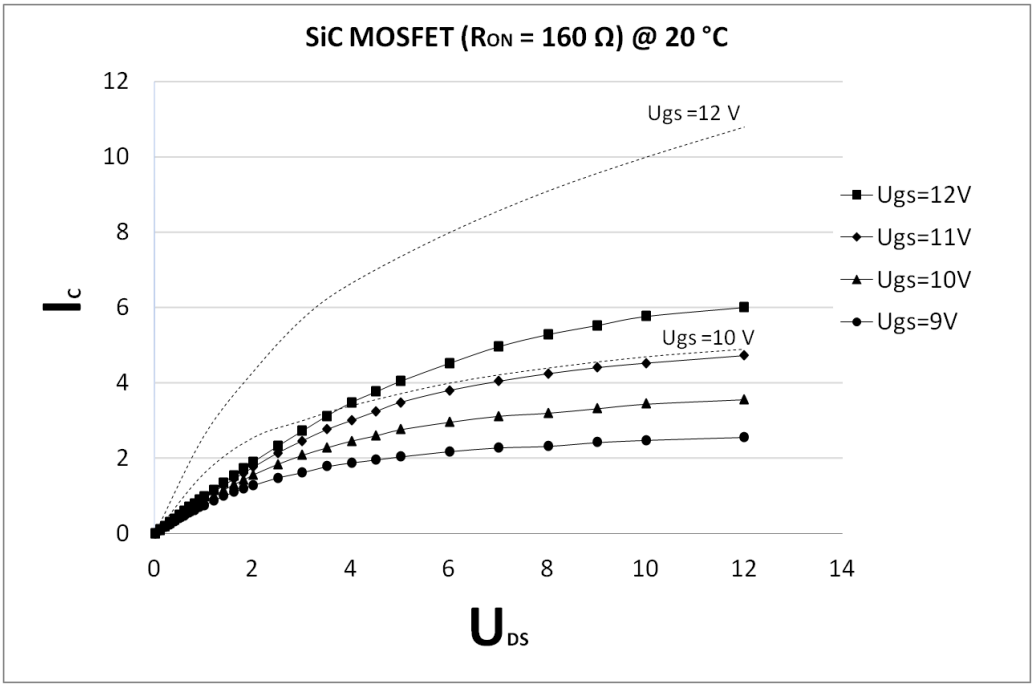

Figure 8: I-V characteristics for a packaged SiC MOSFET (specified as Rdson = 160 mΩ). Data from the manufacturer for Ugs = 10 V and Ugs = 12 V are plotted as dotted lines.

To verify the functionality of the packaged devices we have measured their I-V characteristics. The measurements were made manually using shunt resistances without compensation for resistances in connecting wires, contacts etc. It should be pointed out that this is not an optimal measurement setup and that it does not reflect the I-V characteristics of the devices, but serves only to verify that the I-V characteristics displays linear and saturation regions.

Figures 6 - 8 show the measured I-V characteristics for the SiC BJT and the 80 mΩ and 160 mΩ SiC MOSFETs. Data from the manufacturer are included in the

diagrams for comparison. All devices clearly follow the I-V characteristics of a transistor with linear and saturation regions.

CONCLUSIONS

We introduce a new package design intended for SiC power transistors and operation in high temperatures. The package is a 3-layered sandwich of ceramic substrates and silver die attach. Three types of SiC devices from different manufacturers are packaged and tested in room temperature. Though the devices were still functional after the packaging process, their performance seem to have degraded. This could be a result of the contact plating process or high temperature packaging process but is more likely due to the measurement setup. FEM simulations are also performed to investigate the thermo-mechanical behavior of the package. The target operating temperature of the package is 400 ºC. Modeling show stress concentrations at the corners of the device chip and suggests that this stress is decreased if the substrate metallization is changed from copper to silver.
High voltage breakdown, and protection of the device surface remains to be addressed in future work.
Finally, it should be noted that to achieve high temperature operation of SiC power switches, high temperature passive components are also required.

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