Thermal Modeling of Large Embedded GaN Transistors

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Abstract

This paper highlights the recent thermal characterization and simulation work carried out on large area embedded GaN power transistors. Two types of embedded formats are characterized and compared. A package that has a bottom side thermal pad requires thermal vias is compared, at the system level, with a package that has a top side thermal pad that can be more directly interfaced to a heat sink. In both cases a thermal interface material (TIM) is used to provide electrical insulation. GaN power transistors have $R_{on}{\cdot}Q_g$ Figure of Merit results that are more than 10 times better than SJ MOSFETS. However R_{on} increases substantially as the GaN channel temperature increases. Control of the channel temperature plays a major role in achieving the promised performance improvement expected from GaN devices. It is also vitally important that the heat removal strategies do not compromise the dynamic performance of these exceptional transistors.

Key words: Gallium nitride (GaN), embedded power transistor, thermal interface material

1.0 Introduction

Large GaN transistors that can provide more than 50 A are expected to be introduced this year. Very low inductance packages are needed because the devices can switch in less than 20 ns. Thermal issues normally dictate the general form of the packaging of power transistors. A new system integration approach is required for high speed GaN transistors. System integration planning starts at the device level and it involves the successful combination of a wide range of factors. These are the device packages and their physical constraints, such as footprint and height; and the device electrical parasitic elements, such as inductance and resistance. The embedded lateral GaN devices have the smallest parasitic elements and the package interconnect significantly supplements the current carrying capacity of the GaN die (Figure 1). This study therefore concentrates upon the thermal performance of two variants of the embedded GaN devices. There are two thermal pad location possibilities. The thermal pad - the substrate - can be placed either at the top or at the bottom of the package. The heat removal strategy is closely tied to the positioning of the thermal pad. The electrical performance of GaN transistors is exceptional. They have a Figure of Merit (FOM) 10 times that of SJ MOSFET devices. One of the major factors that provides this performance is the low capacitance that these devices exhibit. It is vital that heat removal strategies do not add excessive capacitance to driven nodes of systems using these devices.

Figure 1: The laminate packaged device shown is a 650 V - 40 mΩ GaN-on-Si e-mode transistor.

1.1 Device Design Strategies

Very high current lateral GaN devices have to be augmented by post processing metal plating strategies. The deposited metal tracks available in conventional process flows are very limited in terms of metal thickness. Electromigration issues and low inductance requirements dictate the use of a post processing strategy. The massive current capability of the GaN transistors allows the delivery of 250 - 500 mA per mm of gate width. Over 2500 mm of gate width can be packed into a 10x10 mm device. The device could therefore potentially deliver 1000 A.

The metal thickness typically offered by foundry services are 1 to 2 µm first metal, and 4 to 5µm second metal. If these were the only metals used, the overall die area would have to be dramatically increased in order to avoid electromigration problems. Very high current lateral

GaN transistors have been described in [1], where electrode plating strategies have been used to thicken the metal tracks. The alternative method described in this paper involves the use of an embedding technique where the package metallization augments the die fabrication metal. In order to assess the cost/benefit of these strategies it is necessary to use relationships that provide simple measures of the potentially effective strategies.

In a previous publication [2] we have provided relationships that allow various device layouts to be compared. The overall area of the device (A), i.e. die size; the current capacity (I_E), i.e. the electromigration, saturation or thermal current limit; the on-resistance (R_{on}); and the voltage specification (V) suitably derated all need to be taken into account. The Device Figure of Merit (DFOM) can be enumerated, for a given voltage rating, using the relationship:

$$\mathrm{DFOM} = I_E/A \cdot R_{on} \qquad \text{Eq.1}$$

In essence DFOM (Eq.1) is the current density per unit of on-resistance for the rated operating voltage of a practical transistor. The performance of the conventional ladder structure can be significantly improved if the metal of a conventional process is plated-up so that a 15 microns total thickness is achieved. This process step is however not available in conventional GaN process flows.

If there is a potential choice between processes, i.e. multiple GaN foundry opportunities, the DFOM relationship is a useful measure. There are at present few foundry choices. A modification of the relationship can be used to allow a device layout topology to be optimized for a given process:

$$\mathrm{LFOM} = I_E \cdot W_g/A \qquad \text{Eq.2}$$

Here in the Layout Figure of Merit (LFOM) (Eq.2) W_g replaces the on-resistance term. Now W_g, the gate width (mm), typically 50-300 mm for a large lateral power GaN power transistor, provides a simple measure of the efficacy of the layout chosen to achieve a given current, within a given overall die area, and for a specified operating voltage. Again I_E must be calculated to meet the electromigration requirements and the area (A) must represent the entire chip area, not just the active area.

These relationships can be used to assess the value of the embedding technique. Example layouts of a GaN device are shown in Figure 2. This is a 650V e-mode device shown without and with the augmented metal system based upon the embedded technique.

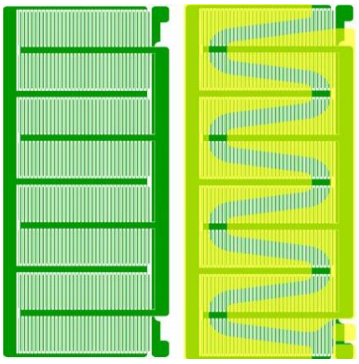


Figure 2: A 650 V e-mode GaN transistor metal structure before and after the embedding process.

The device is rated at 650 V, 34 A - a thermal limit at 100°C, and it has a R_{on} of 40 mΩ at 25 °C. The device area is 14 mm^2 and the W_g is 290 mm. The current rating would have to be reduced to 7.7 A if the embedding process was not used. The DFOM and LFOM values would be 4 times lower. The foundry metal is less than 5 microns thick and it is the electromigration limit rather than the thermal limit that dominates the device current limits.

The ideal device design would have current densities comfortably below even the most conservative electromigration limit - $2 \cdot 10^5$ A per cm^2 for most metals - and near identical thermal and saturation current limits. It therefore important to optimize the thermal conditions because GaN devices have very high intrinsic saturation current limits. The embedding technique has completely removed any electromigration concerns because the package metal augments the metal tracks as shown in Figure 3. The total metal thickness exceeds 30 microns and the critical width is more than 5 times larger.

Figure 3: Embedded device structure.

2.0 Performance Comparison

Embedded power transistors are not commonly available as discrete products. It is therefore appropriate to compare the thermal and electrical performance of the new GaN*PX*™ package devices with established varieties of power transistor packages and other possible technology choices.

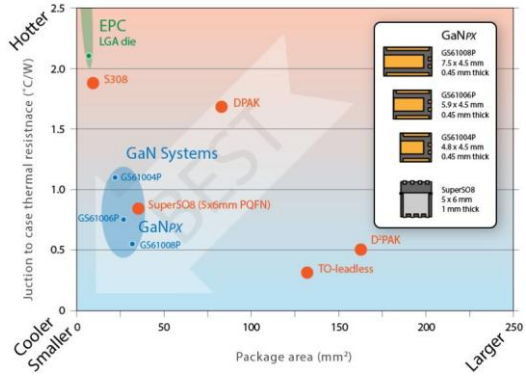


Figure 4: A comparison of package area versus thermal resistance.

The chart shown in Figure 4 compares the thermal performance of standard packages offered by Infineon with the GaN*PX* package. The actual thermal resistance is in all cases partially determined by the chip size and the substrate thickness so the positions shown are approximate. The new package can be seen to comparable with the Super SO8 type. Where a larger GaN die is used, and when the GaN*PX* package with thermal pad on the top is used a further 20-30 % improvement is obtained. Another key measure of usability is related to the extent to which the package adds to the drive loop and other critical commutation path inductances. It is to be expected that "bondless" packages will exhibit the lowest inductance as is shown in the estimates [3] provided in Figure 5.

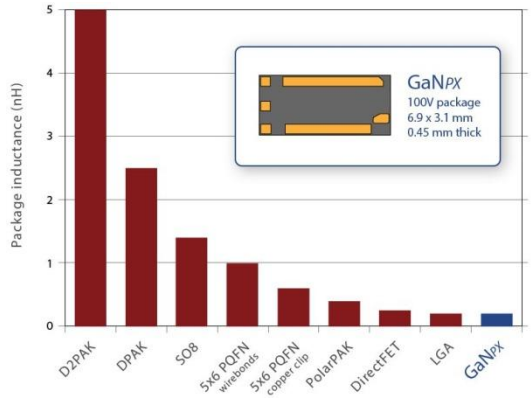


Figure 5: Estimates are shown of the connection inductance of various package types.

All the packages that are small, use clips, or are direct vertical structures, have lead inductances at or below 0.6 nH. The GaN*PX* package with the top heat pad has the lower inductance of the GaN*PX* types. In addition larger chip sizes with wider shorter chips have the lowest inductance. Clips used with wide chips that have been thinned provide the lowest gate drive loop inductance. Where packages, such as the GaN*PX* types, provide a Kelvin source connection the drive issues are greatly reduced and the effect of source electrode inductance is not so pronounced.

Many of these low inductance packages are limited to applications below 200 V because the electrode spacing does not meet the voltage 'creep' distances needed. Higher voltages, such as 650 V, need 2.6 mm or more spacing between the gate/source electrodes and the drain electrode. The high voltage GaN*PX* packages provide the needed 'creep' distance. To bring the critical loop inductance down to or below 0.5 nH, the GaN*PX* package is made to be only 450 microns thick. Further refinements to these packages are planned and low voltage versions that provide even lower inductance, 0.2 nH, as shown in Figure 5, also complete half-bridge circuitry, and integrated drivers can be expected.

The chart shown in Figure 6 compares GaN devices with SJ MOSFETs.

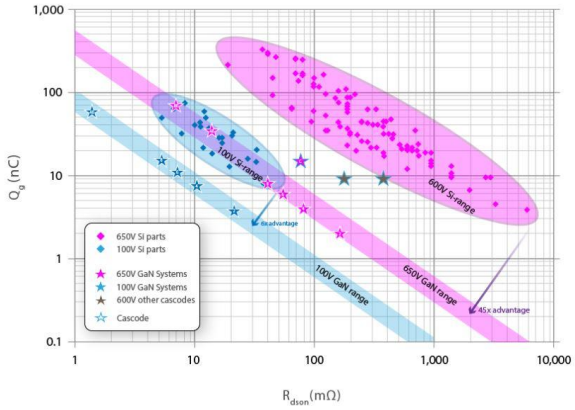


Figure 6: GaN transistors have lower switching charge requirements than SJ MOSFETs for a given specified on-resistance and blocking voltage.

The electrical performance of power devices is difficult to capture in a single set of parameters. Clearly the on-resistance of the device, when used as a switch, is a key parameter. Common practice uses the Q_g vs. R_{on} measure as the factor that most completely determines the value of switch. The

Q_g parameter is a measure of the charge required to switch the transistor on and off. This is easily found on the data sheet of power switching devices. Therefore the Q_g vs. R_{on} chart for a given blocking voltage is an accepted measure of the value of an innovative power switch.

3.0 Thermal Analysis

Thermal performance of two GaN*PX* packages is analyzed. GaN*PX* #1 package has the thermal pad on the bottom of the package as shown in Figure 7 (a).

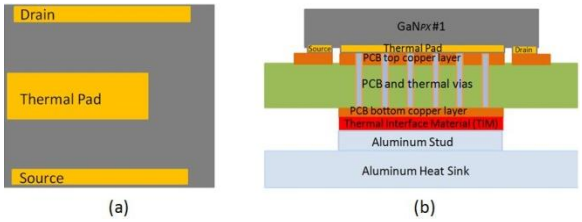


Figure 7: GaN*PX* #1 package: (a) - bottom view, (b) - cross-sectional view of the package mounted on PCB.

The GaN*PX* #1 package requires the use of the several copper layers and thermal vias within the PCB assembly. The cross-section of this assembly is shown in Figure 7 (b). The thermal performance of this package is highly dependent on the PCB structure. Geometric parameters of the PCB are provided in Table 1.

Table 1: PCB geometric parameters.

PCB thickness	1.6 mm
Copper layers thickness	70 µm
Via diameter	0.3 mm
Via array	3x10 and 9x15
Plated Cu thickness in via	35 µm
Aluminum stud height	1 mm

The GaN*PX* #2, which has the heat pad on the top side of the package does not require the PCB vias and it can be connected directly to heat sink using a thermal access stud (Figure 8).

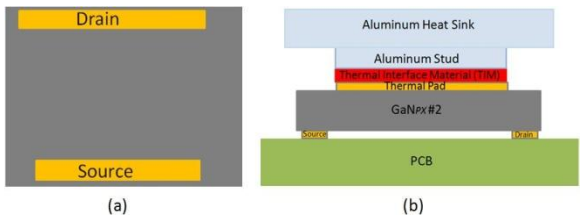


Figure 8: GaN*PX* #2 package: (a) - bottom view, (b) - cross-sectional view.

The electrical insulation between the heat sink and the power devices is required for both packages. Electrical insulation can be achieved by using a thermal interface material (TIM), which is available from several suppliers. Unfortunately TIM has poor thermal conductivity, which is why it is important to take into the consideration the impact of this dielectric layer on device thermal performance. Thermal and electrical characteristics for different TIMs are provided in [4, 5]. Three different TIMs were chosen for this study. TIM thermal parameters are provided in Table 2.

Table 2: Thermal properties of TIM.

Manufacture	Part #	Thickness (mm)	Thermal conductivity (W/m·K)
3M	8810	0.254	0.6
Berquist	GAP 1500R	0.254	1.5
Berquist	GAP 3000S30R	0.254	3

The aluminum heat sink illustrates how a series of access studs can be milled to provide contact to the thermal pad areas of packages (Figure 9).

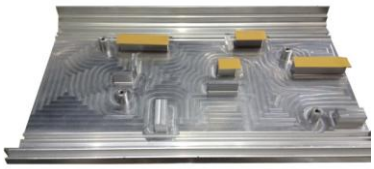


Figure 9: Heat sink milled to provide thermal studs.

In production these studs could be part of a cast heat sink. Alternatively simple impressed indentations can be used in low cost assemblies. The stud, which is made part of a large heat sink, is sized to match the footprint of the thermal pad. Because of the topside mounting of GaN*PX* #2 the stud may need to be several millimeters high to accommodate other components. The impact of the stud height was also investigated in this paper. The height of the stud was changed from 1 mm to 10 mm. The heat sink temperature is held at 50 ^{o}C.

Simplified thermal models for GaN*PX* #1 and GaNPX #2 can be described using the following equations:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta PCB} + R_{\theta TIM} + R_{\theta AlS} + R_{\theta HS} \quad \text{Eq.3}$$

$$R_{\theta JA} = R_{\theta JC} + R_{\theta TIM} + R_{\theta AlS} + R_{\theta HS} \quad \text{Eq.4}$$

where $R_{\theta JA}$ - junction to ambient thermal resistance; $R_{\theta JC}$ - junction to case thermal resistance (package thermal resistance); $R_{\theta PCB}$ - PCB vias thermal resistance for GaN*PX* #1; $R_{\theta TIM}$ - TIM layer thermal

resistance, $R_{\theta AlS}$ - aluminum stud thermal resistance, and $R_{\theta HS}$ - heat sink thermal resistance.

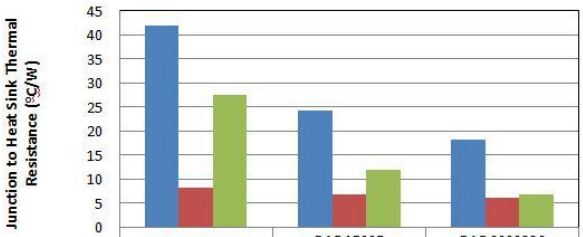
ElectroFlo® (TES International) thermal analysis software was used for this simulation. This is a 3D heat transfer package with Computational Fluid Dynamics (CFD) capabilities, involving conduction, natural and forced convection, radiation, as well Joule heating due to applied electrical bias can be solved self consistently. The coupled thermal analysis type was chosen to define the package junction to case thermal resistance for the simulation. The voltage field was solved in parallel, but coupled to the electrical power dissipation, while including the temperature dependent material properties. The evaluation of this approach was done in [2] and the good agreement between simulation results and measurement was obtained. Both GaN*PX* package variants have the same junction to case thermal resistance, $R_{\theta JC} = 0.5^{o}C/W$.

The assumption was made that the heat sink provides enough cooling to keep the bottom surface of aluminum stud at 50 ^{o}C. Power dissipation was 5W for all thermal simulations. The effect of the stud height was found to be very small.

The GaN*PX* #1 thermal performance is critically dependant on the PCB thermal resistance and characteristics of the TIM. To achieve the best thermal performance PCB and TIM thermal resistance should be optimized. Two PCB designs were used for this purpose: the low thermal conductivity PCB and the high effective thermal conductivity PCB. The first PCB has only two copper layers, which have the same size as the thermal pad, and 30 vias; the second PCB - four copper layers and 135 vias. Source pad and thermal pad were connected for this assembly and a very large TIM pad with a corresponding large area stud was used.

The effects of the TIM thermal conductivity for both packages are shown in figure 10. As expected, according to Equation (4), the impact of TIM's thermal conductivity is very significant for GaN*PX* #2 thermal performance. Increasing the thermal conductivity of TIM from 0.6 to 3 W/m·K decreases the junction to heat sink resistance almost four times. A similar effect occurs for GaN*PX* #1, giving 2.3 times.

The thermal performance of two GaN*PX* is very similar when GaN*PX* #1 is mounted on the high thermal conductivity PCB and the high thermal conductivity TIM is used to connect GaN*PX* #2 to the heat sink (Figure 10).



	3M k=0.6W/m·K	GAP 1500R k=1.5W/m·K	GAP 3000S30 k=3W/m·K
PCB 30 vias	42.01	24.20	18.17
PCB 135 vias	8.172	6.79	6.22
GaNPX #2	27.49	12.06	6.78

Figure 10: Effect of PCB structure and TIM on the GaN*PX* thermal performance.

The GaN transistor die that was used in these simulations is one of eight types. As shown herein there are two package types. There are four die sizes used, one set is intended for 100 V maximum blocking voltage use, the other set for 650 V.

5.0 Conclusion

We have presented two types of embedded GaN transistors. These configurations have merits or demerits that apply in particular applications. The devices with the thermal pad on the top of the package are smaller, have lower loop inductance and are simpler to manufacture. In addition, no PCB vias are required.

However, the package with a bottom mounted heat pad allows for the possibility of using the PCB itself as the heat sink. Where there are few size constraints this package has advantages. The trend is however favoring higher switching speeds and higher current densities so that the dedicated heat sink approach described in this paper will be favored.

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