Redistribution Layers (RDLs) for 2.5D/3D IC Integration

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Abstract
Redistribution layer (RDL) is an integral part of 3D IC integration, especially for 2.5D IC integration with a passive interposer. The RDL allows for fans out of the circuitries and allows the lateral communication between the chips attached to the interposer. There are at least two ways to fabricate the RDL, namely (a) polymers to make the passivation and Cu-plating to make the metal layer, and (b) semiconductor back-end-of-line Cu damascene. In this study, the materials and processes of these methods are presented. Emphasis is placed on the Cu damascene method.

Key words
3D IC integration, through-silicon via (TSV), redistribution layer (RDL), polymer, Cu damascene.

I. Introduction
One of the potential applications of 3D IC integration is wide I/O interfaces [1], which consists of a piece of device-less silicon with through-silicon vias (TSVs) and high-performance, high-density IC chips without TSV. This piece of device-less silicon (also called a passive interposer) is used to support the chips and has RDLs (mainly) for lateral communication between the chips (Figure 1).

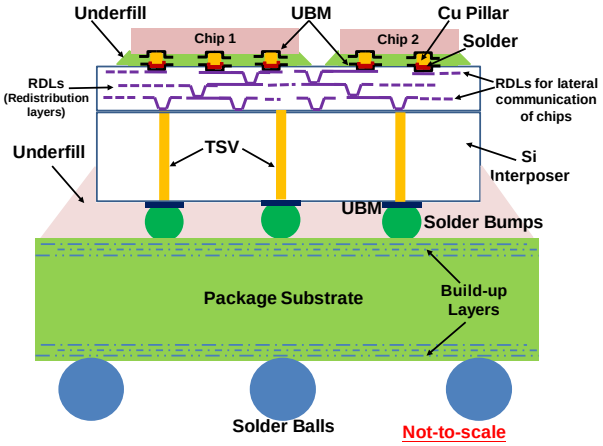

Fig. 1 TSV/RDL passive interposer on substrate

As mentioned in [2, 3], one of the key reasons to have the intermediate substrate (passive interposer) is created by the

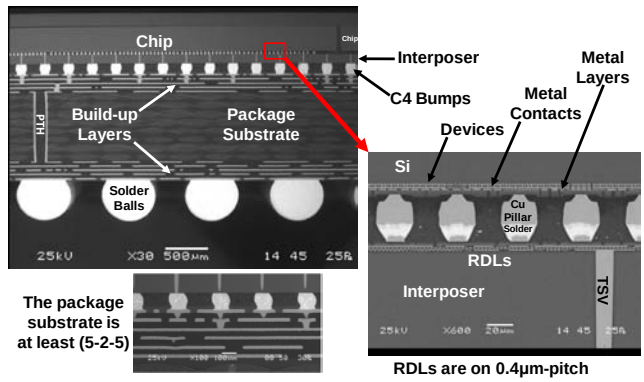

Fig. 2 Xilinx/TSMC's CoWoS

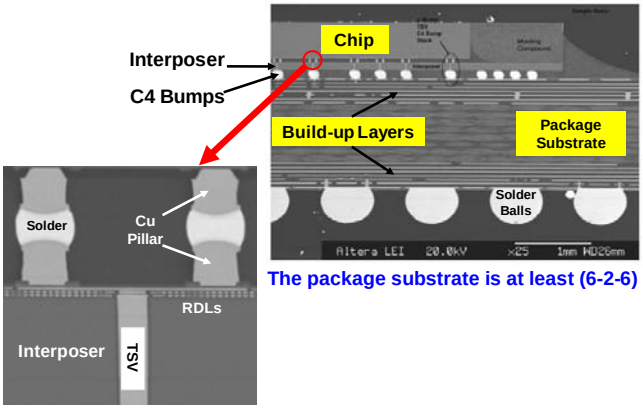

Fig. 3 Altera/TSMC's CoWoS

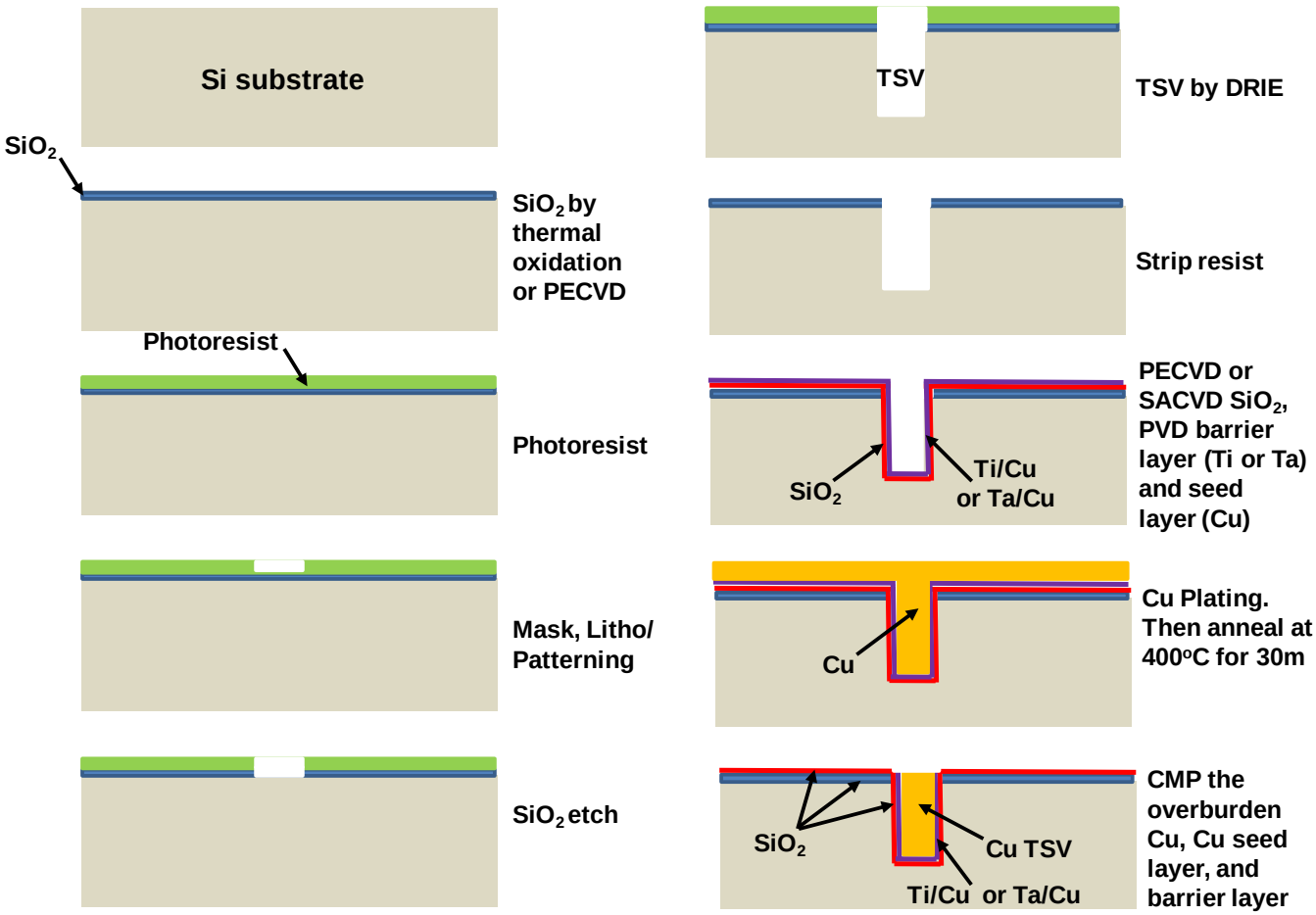

Fig. 4 TSV fabrication process flow

ever increasing IC density and pin-out, and shrinking IC pad-pitch and size, the conventional package substrate cannot support these IC requirements. A couple of examples are shown in Figure 2 (Xilinx/TSMC) [4-6] and Figure 3 (Altera/TSMC) [7, 8]. (CoWoS stands for chip on (interposer) wafer on (package) substrate.) In these cases, it can be seen that even with 12 build-up layers (6-2-6) on the package substrate, it is still not enough to support the FPGA (field-programmable gate array) chips. In addition, a passive TSV interposer with 4 top RDLs (3 Cu damascene layers and 1 aluminum layer) at 0.4μm-pitch is needed. The minimum thickness of the RDLs and passivation is < 1μm. Also, it can be seen that, except for niche applications, passive TSV/RDL interposers are for very high-I/O, high-performance, and high-density applications.

The RDL is the focus of this study. There are at least two ways to fabricate RDLs. One is by using polymers, such as polyimide (PI) PWDC 1000 (Dow Corning), benzocyclobutene (BCB) Cyclotene 4024-40 (Dow Chemical), polybenzo-bisoxazole (PBO) HD-8930 (HD Micro systems), and the fluorinated aromatic AL-X 2010 (Asahi Glass Corporation) to make the passivation layer and electroplating (such as Cu) to make the metal layers. This method has been used by the OSAT (outsourced semiconductor assembly & test) to fabricate RDLs (without using semiconductor equipments) for wafer-level (fan-in) chip scale package [9, 10], embedded wafer-level (fan-out) ball grid array package [11], and (fan-out) redistribution chip package [12]. The other is by using the Cu damascene method which is primarily modified from the conventional semiconductor back-end-of-line to make the Cu metal RDLs as those shown in Figures 2 and 3. In general, much thinner structures (both dielectric layers and Cu RDLs), finer pitches, smaller line-width and spacing can be obtained with the Cu damascene method, which will be emphasis on this study. The polymer/Cu-plating method will be mentioned first. Also, the fabrication of TSV and Cu reveal will be presented.

II. Fabrication of TSV

The fabrication processes of TSVs are shown in Figure 4. It starts with a SiN_x/SiO_x insulation layer by either thermal oxidation or PECVD (plasma enhanced chemical vapor deposition) as shown in Figure 4. After photoresist and TSV lithography, the TSV is etched into the Si substrate by Bosch-type DRIE (deep reactive ion etch) [13] to form a

high-aspect ratio (10.5) via structure. The etched TSV structure is then processed with a SiOx liner by SACVD (sub-atmosphere chemical vapor deposition), a Ta barrier layer and a Cu seed layer by PVD (physical vapor deposition) [14]. Cu electro-plating is used to fill the TSV structure. The final blind TSV has a top opening of approximately 10μm in diameter and a depth about 105μm, which give an aspect ratio of 10.5. In such a high aspect ratio via structure, a bottom-up plating mechanism is applied to ensure a seamless TSV with a reasonably low Cu thickness at the field. The SEM (scanning electron microscopy) cross-section images are shown in Figure 5. It can be seen that the diameter of the TSV is slightly decreased at the bottom, which is expected from the etching process point of view. The Cu thickness at the field is < 5μm. The post-plating anneal is at 400°C for 30 minutes. To complete the TSV process, excess Cu at the field is removed by CMP (chemical-mechanical polishing) [15].

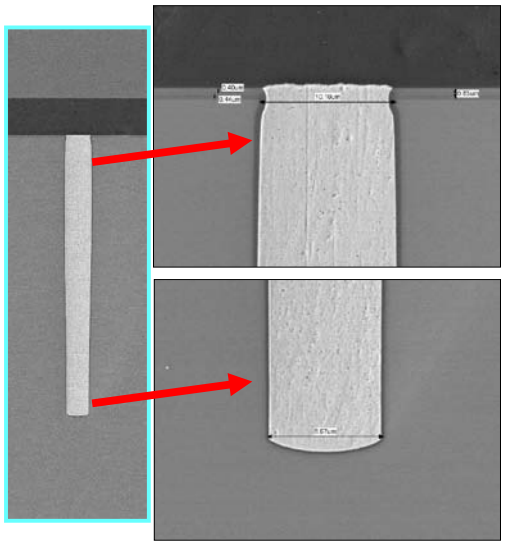

Fig. 5 SEM images of TSV cross sections

III. Fabrication of RDL by Polymers

Continuing with the wafer from Figure 4, the fabrication process for the RDLs using polymers is shown in Figure 6 and also listed as follows. UBM (under bump metallurgy) is included.

Step 1. Spin the polymers such as PI or BCB on the wafer and cure for an hour. This will form a 4 to 7μm thick layer.
Step 2. Apply photoresist and mask, then use photolithography techniques (align and expose) to open vias on the PI or BCB.
Step 3. Etch the PI or BCB.
Step 4. Strip off the photoresist.
Step 5. Sputter Ti and Cu over the entire wafer.

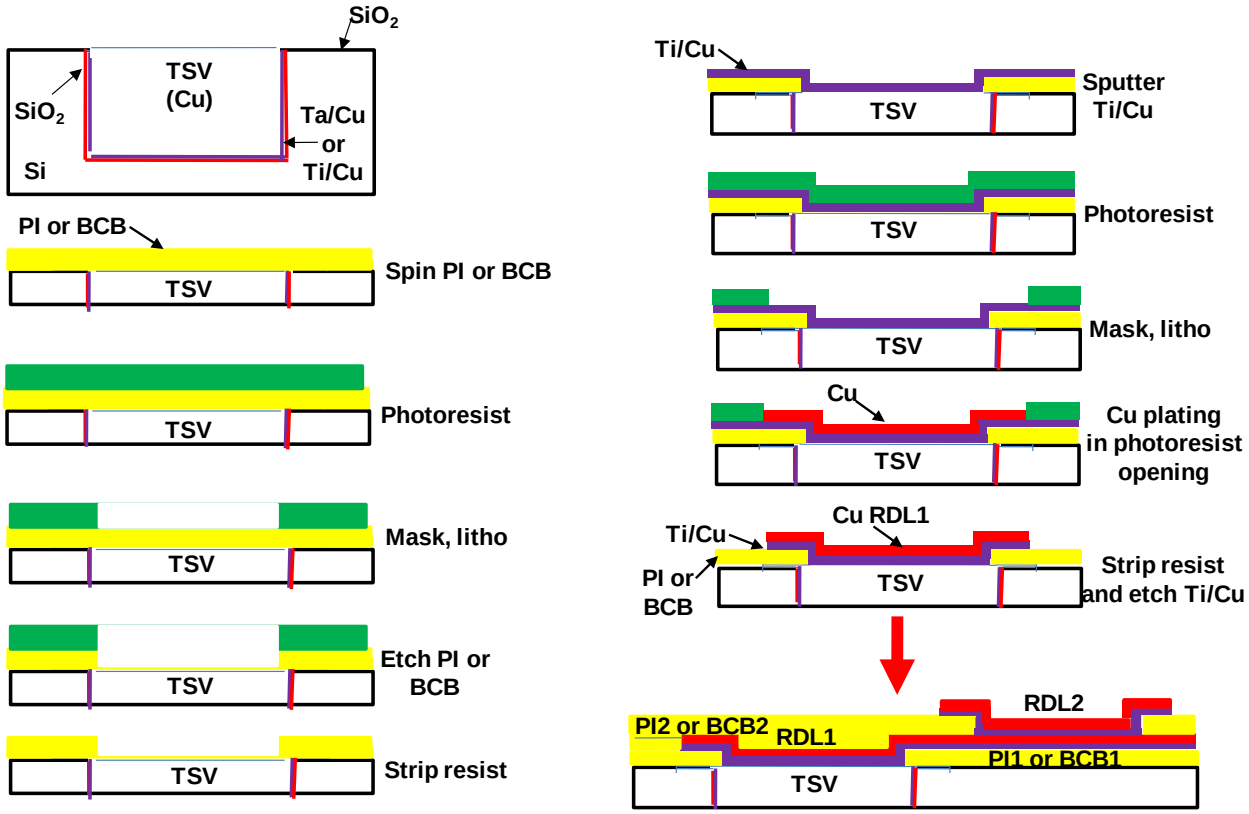

Fig. 6 RDL fabrication process with polymers as passivation and Cu plating as metal layers

Step 6. Apply a photoresist and mask, and then use photolithography techniques to open the redistribution-trace locations.
Step 7. Electroplate Cu in photoresist openings.
Step 8. Strip off the photoresist.
Step 9. Etch off the Ti/Cu and RDL1 is completed.
Step 10. Repeat Steps 1 - 9 for RDL2, and so forth.
Step 11. (For UBM) Repeat Step 1.
Step 12. Apply photoresist and mask, and then use photolithography techniques (align and expose) to open vias on the PI or BCB for the desired bump pads and to cover the redistribution traces.
Step 13. Etch the desired vias on the PI or BCB.
Step 14. Strip off the photoresist.
Step 15. Sputter Ti and Cu over the entire wafer.
Step 16. Apply photoresist and mask, and then use photolithography techniques to open the vias on the bump pads to expose the areas with UBM.
Step 17. Electroplate Cu core.
Step 18. Strip off the photoresist.
Step 19. Etch off the Ti/Cu.
Step 20. Electroless Ni and immersion Au. UBM is completed.

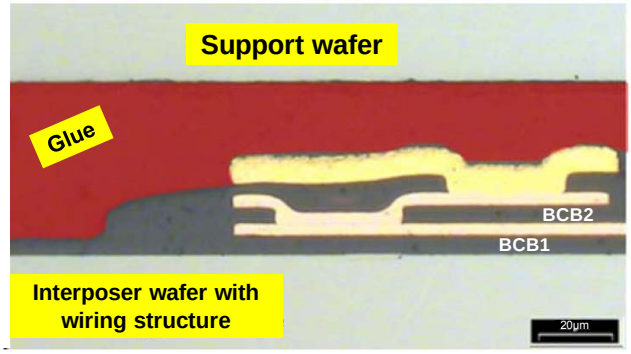

Fig. 7 IZM's RDLs with BCB polymer

A typical cross section of the RDLs with polymers (e.g., BCB) as passivation and Cu plating as metal layers is shown in Figure 7 (IZM's 2 RDLs with BCB1 and BCB2 [16]). It can be seen that the thickness of the passivation layers, BCB1 and BCB2 is about 6~7μm and the RDL is about 4μm.

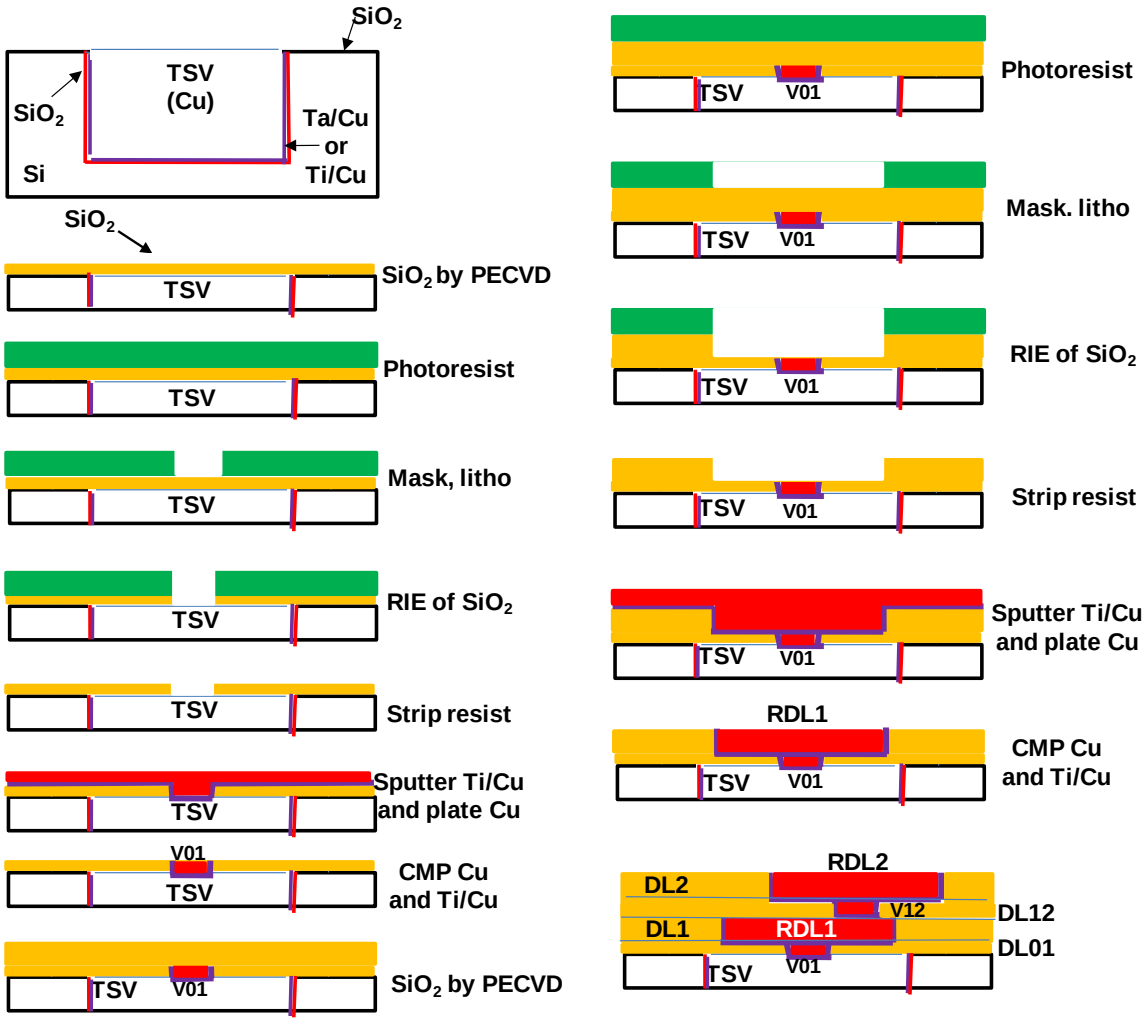

Fig. 8 Process flow of RDLs fabricated by Cu Damascene method

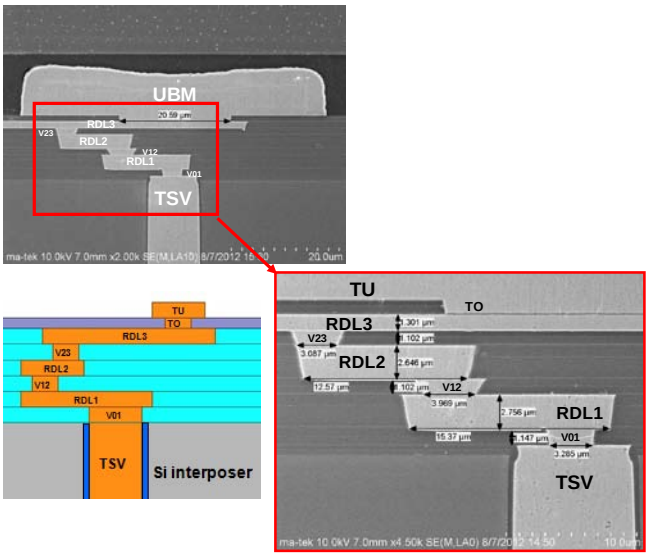

Fig. 9 SEM images of cross sections of RDLs fabricated by Cu damascene method

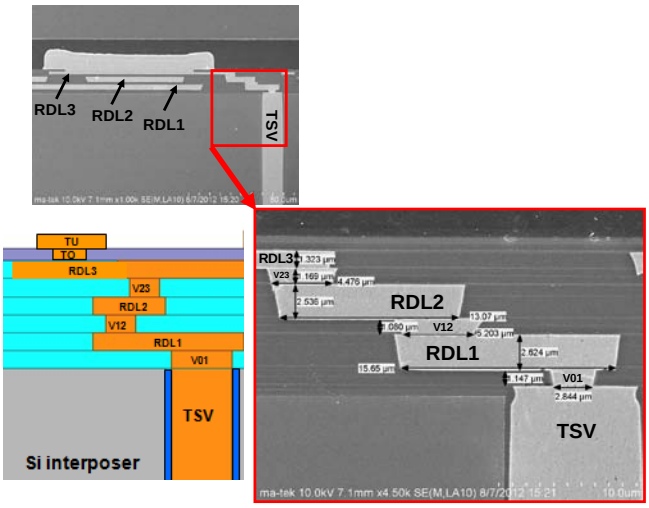

Fig. 10 SEM images of cross sections of RDLs fabricated by Cu damascene method

IV. RDL Fabricated by Cu Damascene

Another method of RDL fabrication is by a Cu damascene process. If starting with the wafer from Figure 4, the fabrication process of RDLs with a Cu damascene technique is primarily based on the semiconductor back-end-of-line process. The details are shown in Figure 8 and listed below.

Step 1. SiO_2 layer by PECVD.
Step 2. Apply photoresist and mask, then use photolithography techniques (align and expose) to open vias on the SiO_2.
Step 3. RIE (reactive ion etch) of SiO_2.
Step 4. Strip off the photoresist.
Step 5. Sputter Ti and Cu and electroplate Cu over the entire wafer.
Step 6. CMP the Cu and Ti/Cu. V01 (the via connecting the TSV to RDL1) is completed.
Step 7. Repeat Step 1.
Step 8. Apply photoresist and mask, and then use photolithography techniques to open the redistribution trace locations.
Step 9. Repeat Step 3.
Step 10. Repeat Step 4.
Step 11. Repeat Step 5.
Step 12. CMP the Cu and Ti/Cu. RDL1 is completed.
Step 13. Repeat Step 1 through Step 6 to complete V12 (the via connecting the RDL1 to RDL2).
Step 14. Repeat Step 7 through Step 12 to complete RDL2 and any additional layers.
Step 15. (For UBM) Repeat Step 1.
Step 16. Apply photoresist and mask, and then use photolithography techniques (align and expose) to open vias on the SiO_2 for the desired bump pads and cover the redistribution traces.
Step 17. Etch the desired vias on the SiO_2.
Step 18. Strip off the photoresist.
Step 19. Sputter Ti and Cu over the entire wafer.
Step 20. Apply photoresist and mask, and then use photolithography techniques to open the vias on the bump pads to expose the areas with UBM.
Step 21. Electroplate Cu core.
Step 22. Strip off the photoresist.
Step 23. Etch off the Ti/Cu.
Step 24. Electroless Ni; immersion Au. UBM is completed.

SEM images of the RDL cross sections fabricated by a Cu damascene technique are shown in Figures 9 and 10. The minimum RDL line-width is 3µm. The thickness of RDL1 and RDL2 is ~ 2.6µm and of RDL3 is ~1.3µm. The passivation thickness between RDLs is ~1µm.

V. A Note on Contact Aligner for Cu Damascene Method

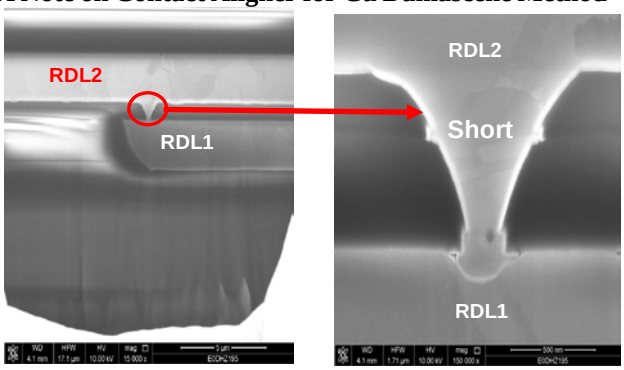

Fig. 11 SEM/FIB showing the short between RDL1 and RDL2. The thickness of the passivation layer between RDL1 and RDL2 is <1µm

The RDLs in this study are fabricated by the Cu damascene method. Lithography using a contact aligner provides a low-cost process as compared to a stepper/scanner under the same resolution requirements. Since the minimum line-width is 3μm in this case, the mask had to be placed very close to the (photoresist) surface of the 300mm wafer. In a few cases, particles on the contact aligner mask punched holes on the photoresist. In this case, shorts may happen such as that shown in Figure 11, which happened while fabricating the V12 (the via connecting RDL1 and RDL2). This can be prevented by cleaning the mask between exposures. Or if cost is not an issue, using a stepper/scanner is another solution.

VI. Backside Processing and Assembly

Some of the backside processes of this wafer (shown in Figure 8) such as the RDLs in the backside have been reported in [17]. The process flow of backside and assembly is shown in Figure 12. It can be seen that after the fabrication of TSV, RDLs, passivation, and UBM, the topside of the interposer wafer is temporary bonded to a carrier by adhesive. It is followed by backgrinding the interposer wafer, Si etching, low temperature passivation, and Cu revealing. Then perform backside RDL (optional), UBM, and C4 (controlled collapse chip connection) wafer bumping. After that, temporary bond another carrier wafer to the backside (with solder bumps) and de-bond the first carrier wafer. It is followed by chip-on-wafer bonding and underfilling. After the whole interposer wafer is completed, then de-bond the second carrier wafer and transfer the thin interposer wafer with attached chips to a dicing tape for singulation. (For thin-wafer handling without temporary bonding and de-bonding, please see [18].) The individual TSV/RDL interposer with chips is attached on the package substrate by natural reflow and then underfilled.

Figure 13 shows more details on Cu revealing. Right after the temporary bonding of the support carrier, it is followed by backgrinding the wafer to a few microns to the TSV, Si dry etching (by RIE) to a few microns below the TSV, and low-temperature passiving the SiN/SiO_2. Then, CMP for SiN/SiO_2 buffing and barrier and Cu seed layers polishing. Cu revealing is completed and shown in Figure 14.

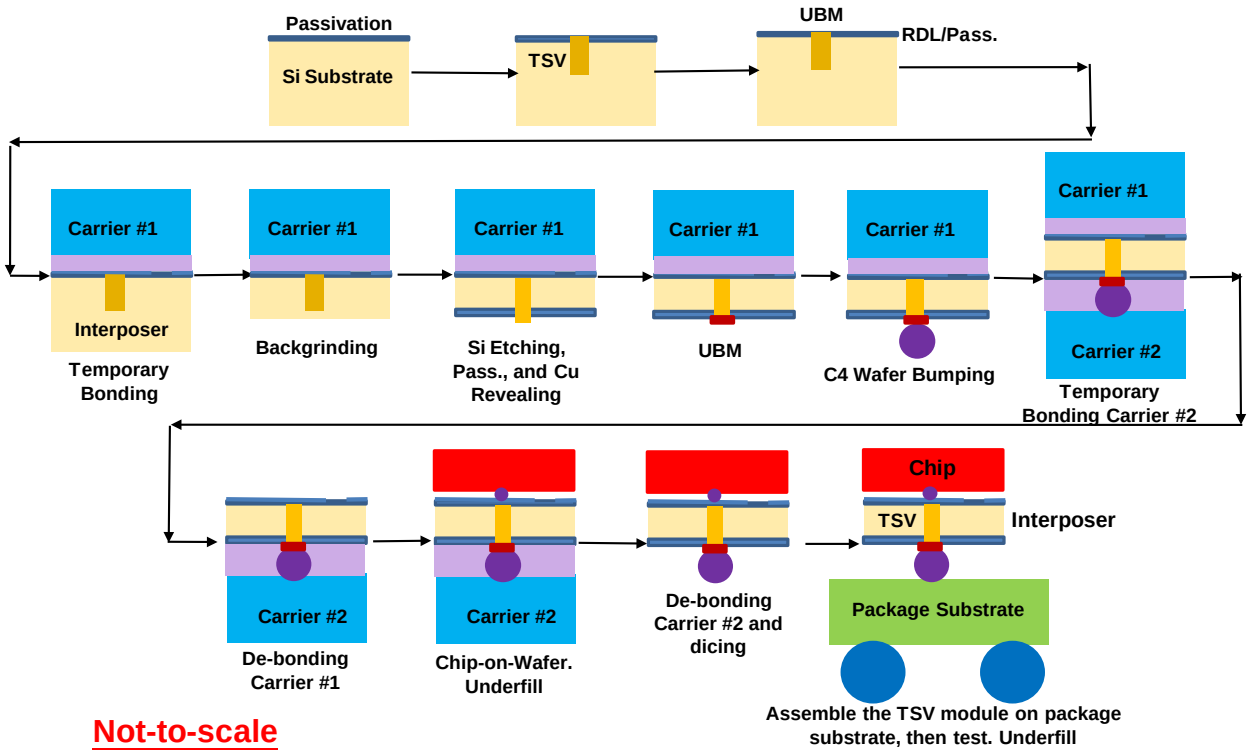

Fig. 12 Conventional process flow for 2.5D/3D IC integration (chip on interposer wafer on package substrate)

VI. Conclusions

The materials and processes for the fabrication of RDLs with two different methods, namely (1) polymer (e.g., BCB) to make the passivation and Cu plating to make the metal layers and (2) semiconductor back-end-of-line Cu damascene have been presented. The fabrications of TSVs, UBMs, and Cu reveal of the interposer have also been described. Some important results and recommendations are summarized as follows.

- The RDLs fabricated by the polymer method are usually thicker. The thickness of the passivation is 6-7μm and the Cu metal layer is 3-4μm.

- The RDLs fabricated by the Cu damascene method are thinner. The thickness of the passivation and the Cu metal layer is ~1μm if a contact aligner is used and in the submicron range if a stepper/scanner is used.
- Lithography using a stepper/scanner can go down to submicron line-width and line-spacing. However, for a few microns' applications, a contact aligner will provide a low-cost process under the same resolution requirements. In order to prevent shorts (not to allow holes in the photoresist and thus the passivation during the fabrication of the vias) between the RDLs, all the particles must be cleaned off from the mask.

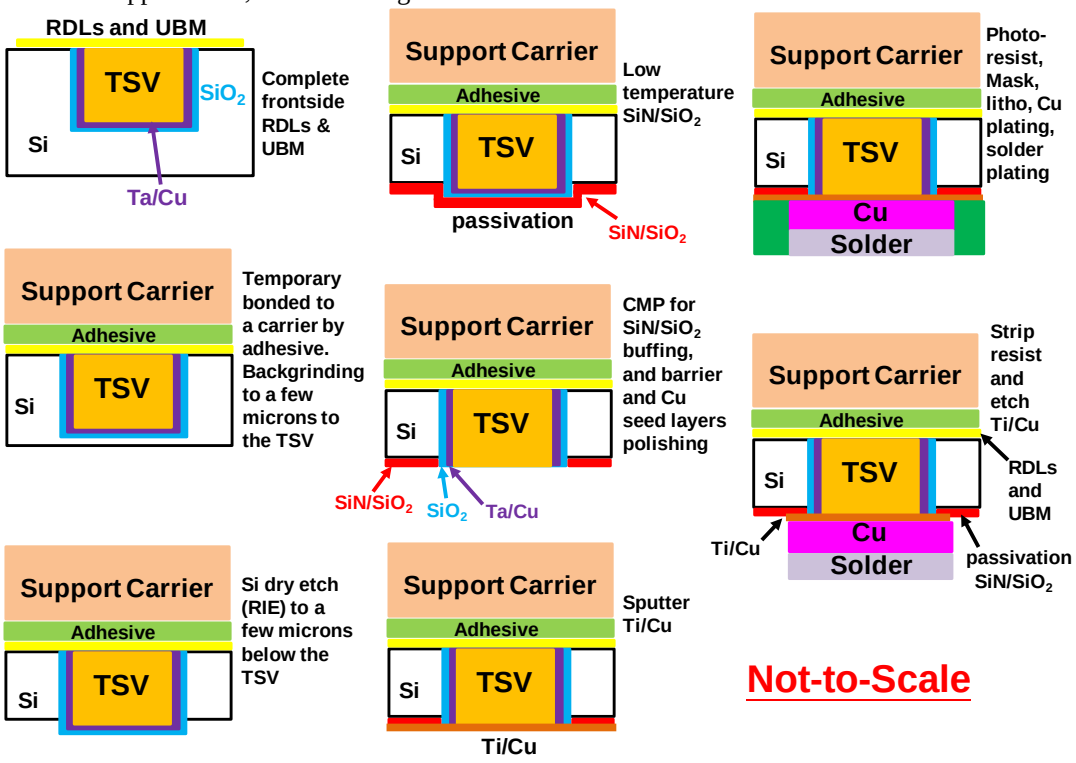

Fig. 13 Backside Cu reveal and UBM/solder plating process flow

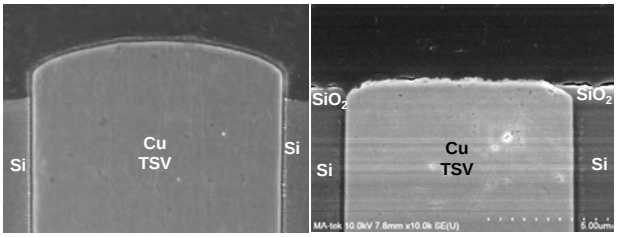

Fig. 14 TSV Cu revealing. (Left) Before dry etch of Si. (Right) After Si dry etching, low-temperature SiN/SiO_2, and removal (CMP) of the isolation, barrier, and seed layer

Acknowledgements

The ITRI authors would like to thank the financial support of Rambus, USA and MOEA, Taiwan. The strong support of the 3D IC Integration program by Dr. C. T. Liu, VP and Director of Electronics & Optoelectronics Research Lab is greatly appreciated.

References

[1] J. H. Lau, *Through-Silicon Via for 3D Integration*, McGraw-Hill Book Company, New York, NY, 2013.

[2] C. Selvanayagam, J. H. Lau, X. Zhang, S. Seah, K. Vaidyanathan, and T. Chai, "Nonlinear Thermal Stress/Strain Analysis of Copper Filled TSV (Through Silicon Via) and Their Flip-Chip Microbumps", *Proceedings of IEEE/ECTC*, Orlando, FL, May 2008, pp. 1073-1081. Also, *IEEE Transactions on Advanced Packaging*, Vol. 32, No. 4, Nov. 2009, pp. 720-728.

[3] X. Zhang, C. Chong, J. H. Lau, C. Selvanayagam, K. Biswas, S. Liu, D. Pinjala, G. Tang, Y. Ong, S. Vempati, E. Wai, H. Li, B. Liao, N. Ranganathan, V. Kripesh, J. Sun, J. Doricko, and C. Vath, "Development of Through Silicon Via (TSV) Interposer Technology for Large Die (21x21mm) Fine-pitch Cu/low-k FCBGA Package", *Proceedings of IEEE/ECTC*, May 2009, pp. 305-312. Also, *IEEE Transactions on CPMT*, 2011, pp. 660-672.

[4] B. Banijamali, S. Ramalingam, K. Nagarajan, and R. Chaware, “Advanced Reliability Study of TSV Interposers and Interconnects for the 28nm Technology FPGA”, *Proceedings of IEEE/ECTC*, Orlando, Florida, June 2011, pp. 285-290.

[5] R. Chaware, K. Nagarajan, and S. Ramalingam, “Assembly and Reliability Challenges in 3D Integration of 28nm FPGA Die on a Large High Density 65nm Passive Interposer”, *Proceedings of IEEE/ECTC*, May 2012, San Diego, CA, pp. 279-283.

[6] B. Banijamali, S. Ramalingam, H. Liu and M. Kim, “Outstanding and Innovative Reliability Study of 3D TSV Interposer and Fine Pitch Solder Micro-bumps”, *Proceedings of IEEE/ECTC*, San Diego, CA, May 2012, pp. 309-314.

[7] J. Xie, H. Shi, Y. Li, Z. Li, A. Rahman, K. Chandrasekar, D. Ratakonda, M. Deo, K. Chanda, V. Hool, M. Lee, N. Vodrahalli, D. Ibbotson, and T. Verma, “Enabling the 2.5D Integration”, *Proceedings of IMAPS International Symposium on Microelectronics*, September 2012, San Diego, CA, pp. 254-267.

[8] Z. Li, H. Shi, J. Xie, and A. Rahman, “Development of an Optimized Power Delivery System for 3D IC Integration with TSV Silicon Interposer”, *Proceedings of IEEE/ECTC*, San Diego, CA, May 2012, pp. 678-682.

[9] J. H. Lau, C. Ouyang, and R. Lee, “A Novel and Reliable Wafer-Level Chip Scale Package (WLCSP)”, *Proceedings of Chip Scale International Conference*, San Jose, CA, September 1999, pp. H1-H9.

[10] J. H. Lau, R. Lee, C. Chang, and C. Chen, "Solder Joint Reliability of Wafer Level Chip Scale Packages (WLCSP): A Time-Temperature-Dependent Creep Analysis," *ASME Paper No. 99-IMECE/EEP-5*, November 1999.

[11] M. Brunnbauer, E. Furgut, G. Beer, T. Meyer, H. Hedler, J. Belonio, E. Nomura, K. Kiuchi, and K. Kobayashi, “An Embedded Device Technology Based on a Molded Reconfigured Wafer”, *Proceedings of IEEE/ECTC*, San Diego, CA, May 2006, pp. 547-551.

[12] B. Keser, C. Amrine, T. Duong, O. Fay, S. Hayes, G. Leal, W. Lytle, D. Mitchell, and R. Wenzel, “The Redistributed Chip Package: A Breakthrough for Advanced Packaging”, *Proceedings of IEEE/ECTC*, Reno, NV, May 2007, pp. 286-291.

[13] Y. C. Hsin, C. Chen, J. H. Lau, P. Tzeng, S. Shen, Y. Hsu, S. Chen, C. Wn, J. Chen, T. Ku, and M. Kao, “Effects of Etch Rate on Scallop of Through-Silicon Vias (TSVs) in 200mm and 300mm Wafers”, *Proceedings of IEEE/ECTC*, Orlando, FL, May 2011, pp. 1130-1135.

[14] C. Wu, S. Chen, P. Tzeng, J. H. Lau, Y. Hsu, J. Chen, Y. Hsin, C. Chen, S. Shen, C. Lin, T. Ku, and M. Kao, “Oxide Liner, Barrier and Seed Layers, and Cu-Plating of Blind Through Silicon Vias (TSVs) on 300mm Wafers for 3D IC Integration”, *IMAPS Transactions, Journal of Microelectronic Packaging*, Vol. 9, No. 1, First Quarter 2012, pp. 31-36.

[15] J. C. Chen, J. H. Lau, P. J. Tzeng, S. Chen, C. Wu, C. Chen, H. Yu, Y. Hsu, S. Shen, S. Liao, C. Ho, C. Lin, T. K. Ku, and M. J. Kao, “Effects of Slurry in Cu Chemical Mechanical Polishing (CMP) of TSVs for 3-D IC Integration”, *IEEE Transactions on CPMT*, Vol. 2, No. 6, June 2012, pp. 956-963.

[16] K. Zoschke, J. Wolf, C. Lopper, I. Kuna, N. Jürgensen, V. Glaw, K. Samulewicz, J. Röder, M. Wilke, O. Wünsch, M. Klein, M. Suchodoletz, H. Oppermann, T. Braun, R. Wieland, and O. Ehrmann, “TSV based Silicon Interposer Technology for Wafer Level Fabrication of 3D SiP Modules”, *Proceedings of IEEE/ECTC*, Orlando, Florida,, May 2011, pp. 836-842.

[17] P. J. Tzeng, J. H. Lau, C. Zhan, Y. Hsin, P. Chang, Y. Chang, J. Chen, S. Chen, C. Wu, C. Lee, H. Chang, C. Chien, C. Lin, T. Ku, M. Kao, M. Li, J. Cline, K. Saito, M. Ji, “Process Integration of 3D Si Interposer with Double-Sided Active Chip Attachments”, *Proceedings of IEEE/ECTC*, Las Vegas, NV, 2013, pp. 86-93.

[18] J. Lau, H. Chien, S. Wu, Y. Chao, W. Lo, and M. Kao, “Thin-Wafer Handling with a Heat-Spreader Wafer”, *Proceedings of IMAPS International Symposium on Microelectronics*, September 2013, Orlando, FL. (In this proceedings.)