Chip Package Interaction: Understanding of Contributing Factors in Back End of Line (BEoL) Silicon, Cu Pillar Design and Applied Process Improvements

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Abstract

This paper describes major contributing factors to the CPI risk and reveals the mitigation strategy successfully applied jointly by GLOBALFOUNDRIES as the silicon supplier and Qualcomm Technologies, Inc., as the customer responsible for packaging. This strategy involves thermo-mechanical modelling, data collection on wafer level using shear test to assess the BEoL-stability, Cu Pillar process development and optimization. The qualification of these process changes had been completed and implemented in volume production.

The paper also discusses mechanical wafer level and thermo-mechanical package modeling approaches. A model has been applied to determine the critical factors on BEoL stress/strain during the flip-chip assembly reflow process. These factors include for instance the Cu Pillar bump geometry and stack up. The results of the modelling work were used to set up experiments to further mitigate CPI related failure modes in BEoL on the package level.

GLOBALFOUNDRIES and Qualcomm Technologies, Inc., assessed Cu Pillar design related rules such as Cu Pillar diameter and height as well as the Cu Pillar stack up. Process improvements were carried out to reduce the undercut of the barrier underneath the Cu Pillar. The paper reveals how effectively an optimized Cu Pillar design and improved Cu Pillar processing can contribute to the risk mitigation of CPI failure modes in the BEoL for critical package designs and assembly processes with low margin against BEoL fracture during solder reflow.

Furthermore, process improvements applied to enhance the BEoL stack strength were investigated and have been implemented in high-volume production. A strong correlation was established between data collected on wafer level to assess the BEoL strength and data collected on package level.

Key words

Chip-Package Interaction, Cu Pillar, Bumping Process, Thermo-Mechanical Modeling, Shear Test

I. INTRODUCTION

The initiation of cracks in the brittle ultra low-k dielectric material in the Back End of Line (BEoL) on advanced node silicon devices is of major concern for assembly processes [1-4]. It is attributed mainly to various combinations of the Chip-Package-Interaction (CPI) effects. This challenge is further amplified by the adoption of Cu Pillars to replace conventional solder bump flip chip interconnects as the device bump pitch shrinks and the demand for higher I/O counts per area soars. Furthermore, the adoption of Cu Pillars as interconnects is inevitable because Cu Pillars offer superior electrical performance. The high modulus and yield strength of Cu can transfer significantly higher thermo-mechanical stress to the ultra low k layer and increases the risk of dielectric cracks. It is therefore important to understand the CPI challenges of Cu Pillars on ultra low k chips in detail, and more importantly to turn all possible knobs to mitigate the risk of package induced failure modes in the BEoL.

Fig. 1 depicts the main contributing CPI risk factors, which are related to the silicon (i.e. BEoL stack and design rules, processing of the silicon) the interconnect material and design rules (i.e. SnAg bumps, Cu Pillar), the assembly technology (FC-CSP, FC-BGA, wafer level packaging), the assembly material and the substrate or board design.

The broad spectrum of impacting factors is depicted in Fig. 1 and had been described in detail previously [5].

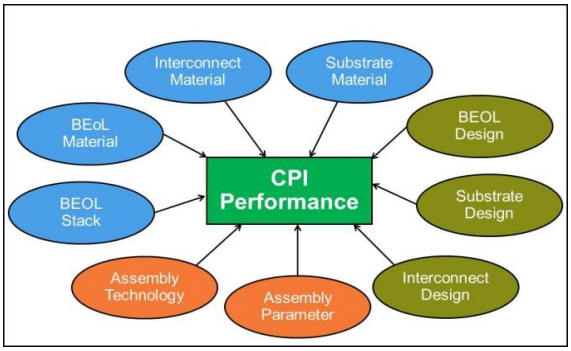

Fig. 1: Main contributing CPI risk factors

This paper concentrates on the impact of Cu Pillar design and Cu Pillar bumping process improvements as well as the contribution of BEoL process optimization, which is summarized under the terms “Interconnect Material”, “Interconnect Design” and “BEoL Material” in Fig.1.

II. FINITE ELEMENT MODEL

II. A. Thermo-mechanical modeling

A multi-level package modeling technique is used to verify the experimental data with respect to under bump metallization (UBM) diameter and Cu Pillar height variations. This modeling technique is already well described in a previous publication [6]. It is to be noted that a chip package interaction (CPI) failure that is usually observed in BEoL occurs within the ultra low-k (ULK) levels under the bump, which is where the maximum ULK strain is observed in the simulation model as depicted in Fig.2.

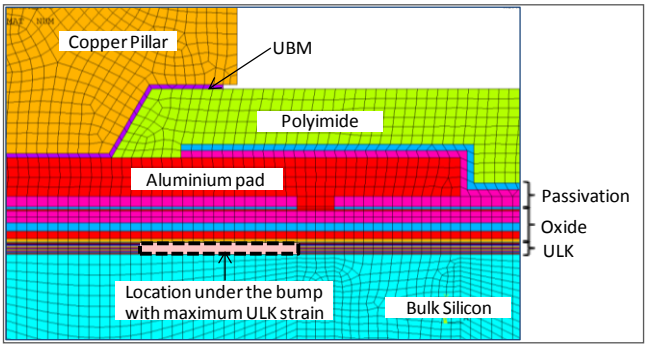

Fig. 2: Local model showing the location of maximum ULK strain

For the first case study the UBM diameter is varied between 46µm to 50µm as seen in Fig.3. The strain in the ULK level decreases consistently as the UBM diameter increases. The ULK strain is reduced by 5% and 8% when the UBM diameter increases from 46µm to 48 and 50µm respectively.

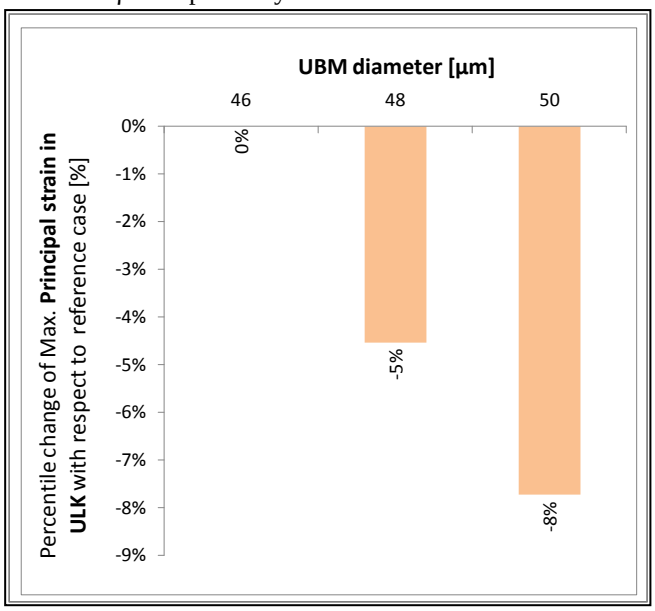

Fig. 3: Effect of UBM diameter on the maximum principal strain in ULK. Percentile change in ULK strain with respect to first case as reference

The second case studies the effect of Cu Pillar height variation from 30µm to 35µm on the maximum strain generated in the ULK. The maximum principal strain in ULK increases by 3% with 35µm Cu Pillar height as compared to 30µm Cu Pillar as depicted in Fig.4. In addition, Fig.5 shows that the area of the maximum ULK strain is increased with 35µm Cu Pillar height as compared to 30µm Pillar.

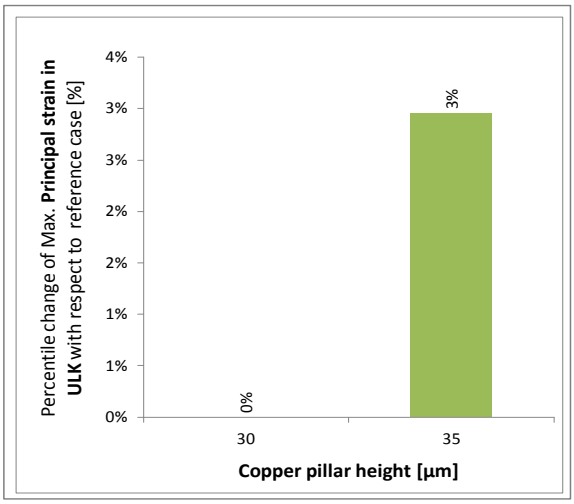

Fig. 4: Effect of Cu Pillar height on the maximum principal strain in ULK. Percentile change in ULK strain with respect to first case as reference.

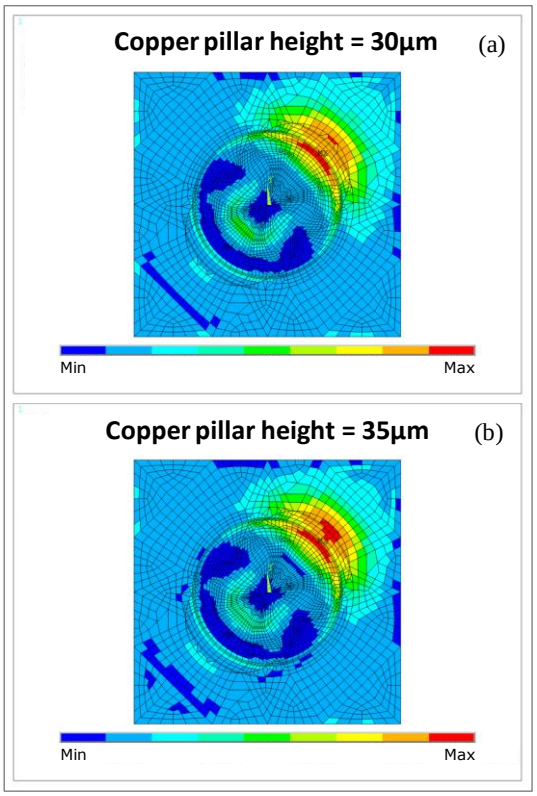

Fig.5: Principal strain plots at ULK level (a) with 30µm Cu Pillar height (b) with 35µm copper pillar

II. B. Mechanical modeling

The single bump shear modeling technique, known as bump assisted back end of line stability indentation (BABSI) simulation, is used to check the effect of the UBM undercut on under bump BEoL stability with different UBM diameters. This modeling technique employed was also described previously [7].

In Fig. 6, the UBM undercut has been varied between 0 and 2µm for cases with UBM diameters varying between 40 to 80µm. Here again it is seen that the larger UBM diameter causes lower ULK strain irrespective of the UBM undercut. Furthermore, larger UBM undercuts consistently lead to higher strain in the ULK for all considered UBM diameters.

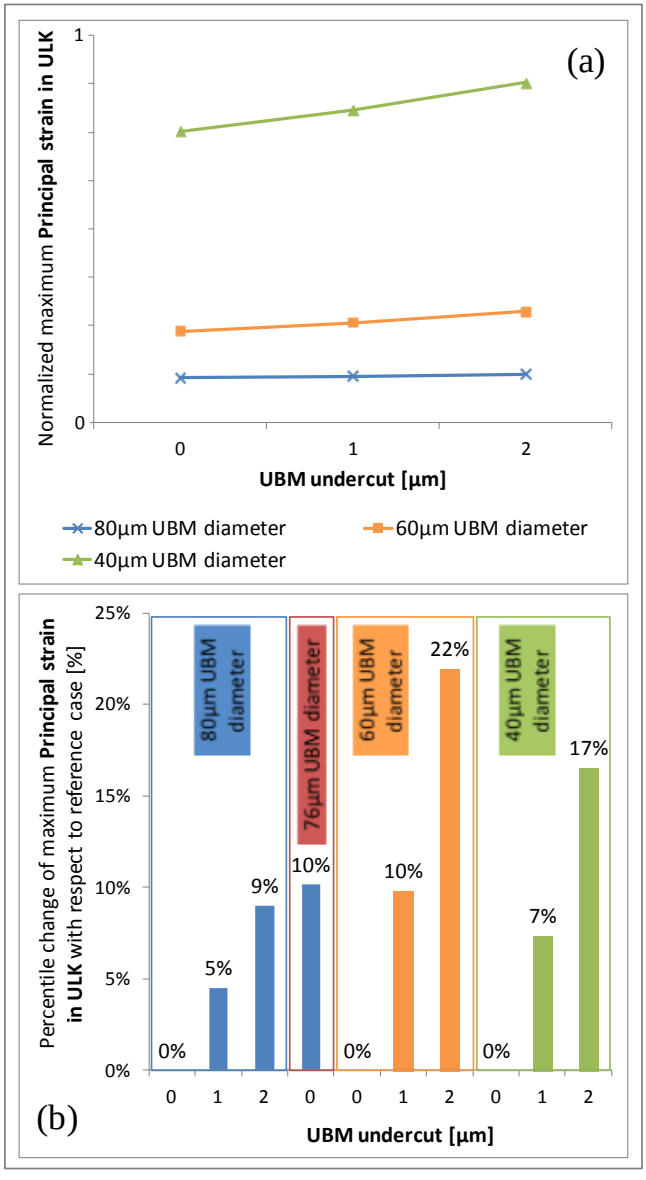

Fig.6: Effect of UBM undercut together with UBM diameter on the maximum principal strain in ULK (a) Normalized ULK strain values (b) Percentile change in ULK strain with respect to reference case.

The above results indicate that the effect of the UBM undercut is the lowest for a large UBM diameter of 80µm. The effect of the UBM undercut increases substantially with smaller UBM diameters, as long as the UBM diameter is significantly larger than the polyimide opening. As shown in Fig. 6~~.~~, the effect of the UBM undercut is less for the 40µm UBM diameter than for the 60µm UBM diameter. This is because the UBM landing on polyimide with 40µm UBM diameter is very close to the polyimide opening of 30µm, which is considered in the model. Therefore, the shear load coming from the Cu Pillar is not so strongly absorbed by the small UBM area over the polyimide, but is transferred through the polyimide opening onto the aluminum pad and from there into the BEoL stack. Hence the ULK strain for the 40µm UBM diameter is significantly higher than for the 60µm UBM diameter and the UBM undercut effect for the 40µm UBM diameter is slightly reduced as compared to the 60µm UBM diameter.

Moreover comparing the 80µm UBM diameter and 2µm UBM undercut to a 76µm UBM diameter and 0µm UBM undercut shows, that the UBM undercut has the same influence on the strain generated in the ULK as a smaller UBM diameter.

III. A. Assessment of Cu Pillar Design and Process Improvements

As shown by simulation, the UBM diameter has the strongest impact compared to the Cu Pillar height. The diameter is considered to be effectively changed by the undercut. However, the solder cap height and the solder joint formation which is not considered within the shear test and shear test simulation, contribute significantly to the stresses which can be transferred into the BEoL.

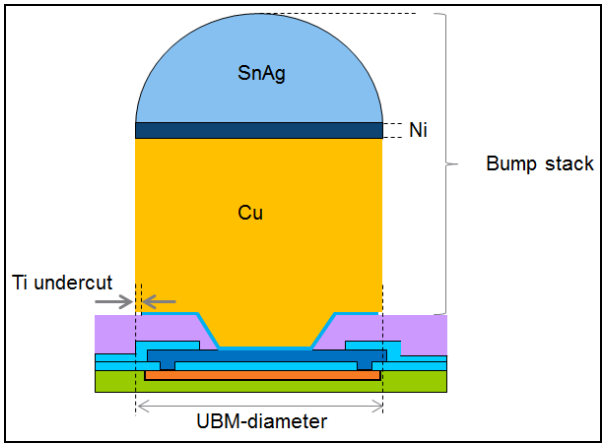

Fig.7: Definition of bump dimensions

The size of the UBM diameter determines the size of the contact area between the bump and the BEoL stack. The mechanical force that is exerted at the bump is distributed across the UBM area and is creating mechanical stress in the BEoL layers. The larger this

area is, the better the mechanical stress can be distributed. Hence, increasing the UBM diameter will reduce the stress in the BEoL layers and therefore reduce the risk of ULK cracking (see modelling results in Fig.6).

Another very important factor is the bump stack itself. A typical bump Cu Pillar stack consists of three layers: Cu, Ni, SnAg. Typically, the thickness of the Ni layer is not varied very much because it functions as diffusion barrier and requires a certain thickness which is independent of the heights of the Cu and the SnAg cap.

The Cu height however, can be varied. The Cu height should be as small as possible to reduce stress coming from the substrate into the BEoL. The higher the Cu is, the stronger the torque will be that the mechanical forces induce at the interface of the Cu Pillar to the BEoL (Fig.8, see also modelling results in Fig. 5).

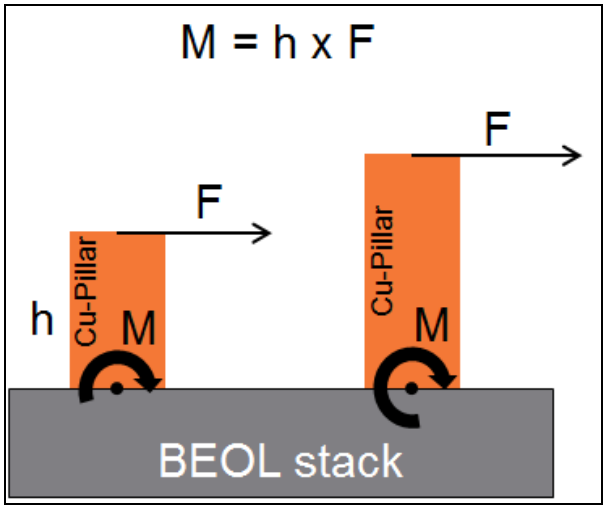

Fig.8: Impact of Cu Pillar height on BEoL

On the other hand, a minimum Cu height is needed to ensure the required distance between the silicon die and the substrate in the package is met. A reduction of this stand-off distance is limited by the ability of the molding or underfill processes to fill the gap properly.

The size of the SnAg cap can also be used to reduce the stress in the ULK layers. The more solder volume can be brought into the gap between substrate landing pads and the Cu Pillar the more strain it can absorb. However, there are limitations, which must be taken into consideration. Very important is, that the solder is kept between Cu Pillar and landing pad and that it is not completely transformed into an intermetallic compound (IMC). If the solder is wetting the Pillar sidewall, higher stress will be induced on the silicon and the effective volume of the solder, which can absorb stress by plastic strain, is reduced. Hence, a balance needs to be found for the SnAg cap height.

III. B. Assessment of Cu Pillar Bump Process

Modelling results determined the directions of bump process adjustments, which were later successfully implemented in production.

The final UBM diameter can be influenced by several process parameters in the bump flow. The most obvious is of course the size of the bump diameter, determined by the reticle. Furthermore, bump lithography parameters have to be evaluated. By choosing different focus and dose settings at bump exposure, the via size and shape of the bump resist can be adjusted within certain limits. The definition of the via in the resist has to be considered as it determines the geometry and shape of the Cu Pillar. In addition, the diameter of the UBM is reduced by the following UBM etch processes. Fig. 9 depicts major bump process, which can be adjusted to minimize CPI related failures in BEoL.

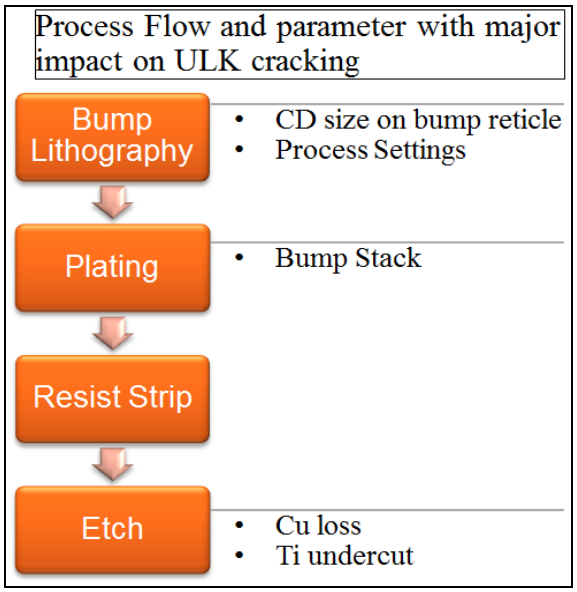

Fig.9: Process flow and parameter with major impact on BEoL stability

The standard UBM stack consists of Ti and Cu. When the UBM is etched, especially in the Cu etch step the Cu Pillar will also be attacked. The Cu loss can be significantly greater than the actual Cu thickness in the UBM layer. A balance in the process has to be found between the complete removal of the UBM and limiting the Cu loss.

The Ti etch step is another important factor and the current process uses a standard chemistry, which causes a larger undercut. Initially, a standard chemistry combined with an additional anisotropic etch step was used to remove the Ti. Even though the Ti undercut was reduced significantly, the overall results were not sufficient. Therefore, a new Ti etch process was developed with a different chemistry to further reduce the undercut. The improvements made are depicted in Fig. 10.

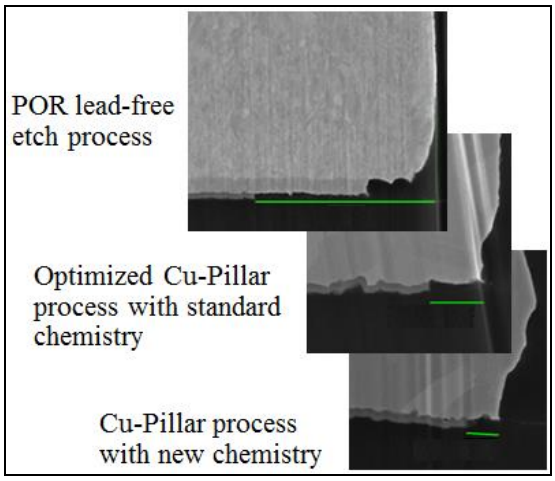

Fig. 10: Reduction of UBM undercut by process optimization

III. C. Assembly Results

The final criteria for process changes based on theoretical assumptions and wafer level testing are the assembly results for actual packages and products which are presented in the following section.

The first example describes the optimization of bump lithography settings. A split lot was executed and the modelling results were verified. The process change increased the UBM diameter by less than 5 %. At the assembly level, this change leads to a significant reduction of yield loss (Fig. 11).

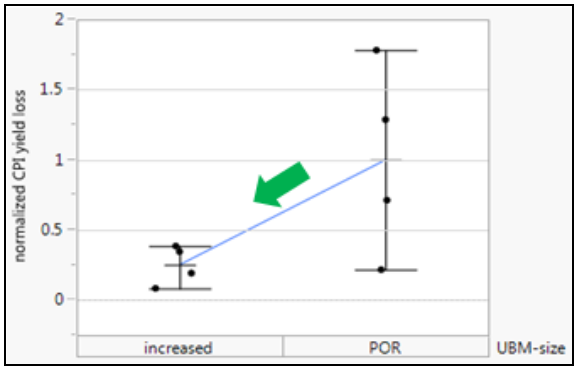

Fig. 11: Reduction in yield loss due to ULK cracking by less than 5% increased UBM diameter

Another split has been performed to check the effect of a reduced Cu height. A significant improvement in yield loss had been observed and the prediction made by modeling had been verified.

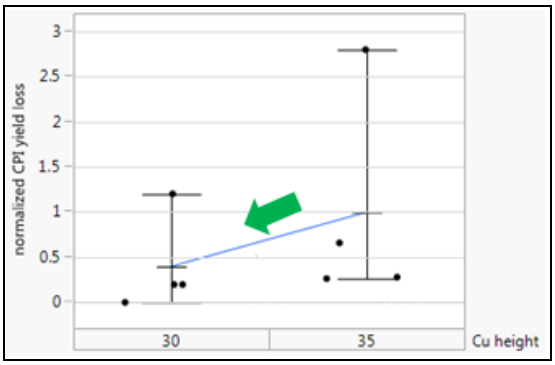

Fig.12: Reduced Cu height leading to less ULK cracking fails

Finally, an optimized process with respect to bump lithography settings and bump stack has been rolled out to production. Yield losses, which were attributed to ULK cracking at different assembly sites, were reduced drastically as seen in Fig. 13.

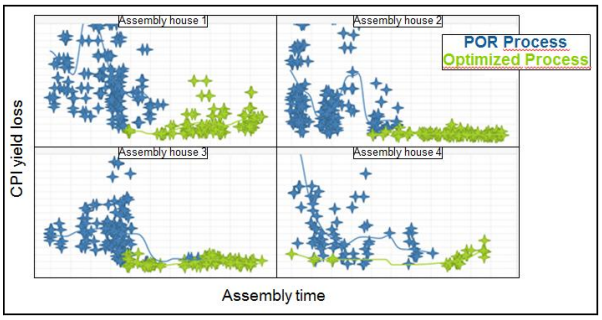

Fig.13: Assembly T0 yield – comparison of POR and optimized Cu Pillar process

IV. BEoL Stack Characterization – BABSI / SPST

Ultralow-*k* (ULK) and low-*k* interlayer dielectric (ILD) films are the mechanically weakest materials in BEoL layer stacks. Extensive engineering work is required to strengthen the interfaces between these ULK or low-*k* films and the adjacent passivation layers. At the end, both cohesive and adhesive strength must be sufficient so that the brittle films withstand CPI stresses acting on the BEoL layer stack without initiating flaws or cracks. The choice of suitable ILD precursors as well as UV curing predominantly influence the overall strength of the brittle ILD films, keeping the tradeoff between lowest possible dielectric permittivity and highest possible mechanical strength in mind. On a real product wafer with a multi-level Cu/low-k/ULK BEoL layer stack, further parameters like local metal densities and design related influences come into play. In this context, local mechanical probing methods are used to experimentally assess the strength of structured multi-level Cu/low-k/ULK BEoL

layer stacks on wafer level. The respective BABSI test and Single-Pillar Shear Test (SPST) techniques have already been described elsewhere [8]-[9]. BABSI and SPST are applied to individual die contacts, which currently consist of Cu Pillars. Depending on the desired loading condition, a pyramidal diamond probe is brought into contact with a single Cu Pillar at its top surface (BABSI test), or a wedge shaped probe approaches the sidewall of the pillar (SPST), followed by shear displacement at a predefined and feedback controlled height above the surface of the die. One unique feature of these techniques is that they can be applied to virtually all pillar positions on a silicon die, especially on critical areas like die corners where the highest CPI stresses are suspected. The failure mode obtained after shear testing on an individual die contact is classified by means of the shape of the respective load-displacement curve $F_x(X)$. A crack propagating inside the BEoL layer stack leads to an abrupt drop ΔF_x of the lateral force at a well-defined lateral displacement $X = X_{crit}$. This is due to the brittle fracture of low-*k* or ULK films inside the BEoL stack. On the other hand, if the BEoL layer stack is stable all over the shear test until $X = X_{max}$ is reached, the $F_x(X)$ curve looks smooth. In this case, there is only plastic deformation of the Cu Pillar and the Al pad, or the pillar detaches from the contact pad. Such fails are not classified as BEoL fails here. They are called far BEoL (fBEoL) fails to differentiate them from cracks inside the BEoL stack. No critical quantities are reported for fBEoL failure modes since there are no well defined abrupt events in the $F_x(X)$ curves. The BEoL stack at test sites with fBEoL failure modes is classified as being more stable than any site with brittle BEoL crack events, i.e., fBEoL fails are treated like "no BEoL fail". Failure modes were additionally verified by optical inspection. The number of BEoL cracks identified in this way per total number of tests results is the BEoL fail rate for a certain wafer for the chosen test condition.

The BEoL fail rates for three different wafers obtained from SPSTs are shown in Fig. 14. Several dies from the wafer center, wafer edge and half the distance between center and edge were investigated on each wafer using a height of $Z = 24\mu m$ of the probe apex above the surface of the die. The average height of the Cu Pillars was $h \approx 50\mu m$. For SPSTs, the same locations of the die contacts were chosen for all samples. The die contacts consist of oblong (oval with a flat long side) Cu Pillars with their orientation of the long pillar axis being adapted to the location on the die. SPSTs were conducted at 0deg, 45deg and 90deg shear direction relative to the long pillar axis to investigate the influence of the direction of the applied in-plane stress on the BEoL stability beneath the die contacts.

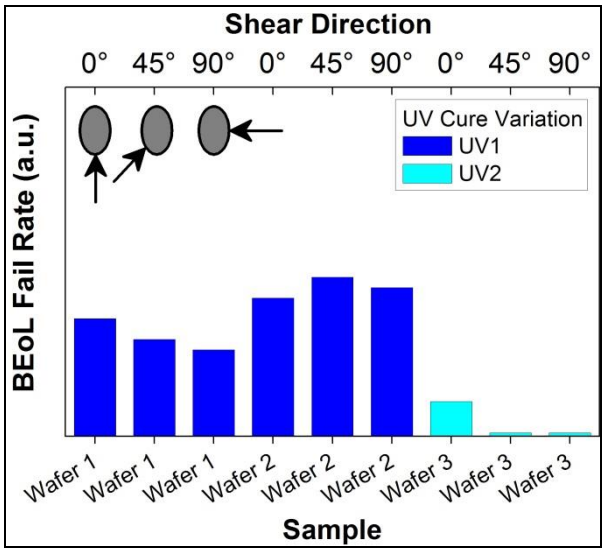

Fig. 14: BEoL fail rates obtained on different wafers using SPSTs at 0deg, 45deg and 90deg shear direction. The BEoL layer stack on wafer 3 was processed with a different UV cure as compared to wafers 1 and 2.

The first measurement series for each wafer in Fig. 14 contains all data for 0deg, the second for 45deg and the third for 90deg shear direction. The main outcome of this study is an overall BEoL fail rate, which is higher on wafers 1 and 2 as compared to wafer 3. Wafers 1 and 2 on the one hand and wafer 3 on the other hand are different with respect to the UV curing process within the BEoL stack (UV1 vs. UV2). The difference between UV1 and UV2 is the position in BEoL processing, when the UV cure process is carried out. All other fabrication parameters remained the same. This leads to the conclusion that the UV2 process makes the BEoL layer stack stronger than UV1. Consequently, wafers with UV2 will be mechanically more stable with respect to CPI stress.

Critical strain energy values were quantified by computing the integral $\int F_x dx$ between $X = 0$ (start of lateral motion of the shear test) and $X = X_{crit}$ (at the first critical event, e.g. force jump, on the $F_x(X)$ curve). The results depend on the shear direction and on the UV cure process as indicated in Fig. 15. The highest critical strain energy for BEoL failures on wafer 1 is detected for 0deg shear, followed by 45deg and 90deg, respectively. The same trend is observed for wafer 2, which was processed in the same way as wafer 1. This demonstrates the repeatability of the method. A comparison of the mean critical strain energies for a certain shear direction reveals slightly lower values for wafer 2 compared to wafer 1. This is consistent with slightly higher BEoL fail rates on wafer 2, probably due to a slightly higher defectivity.

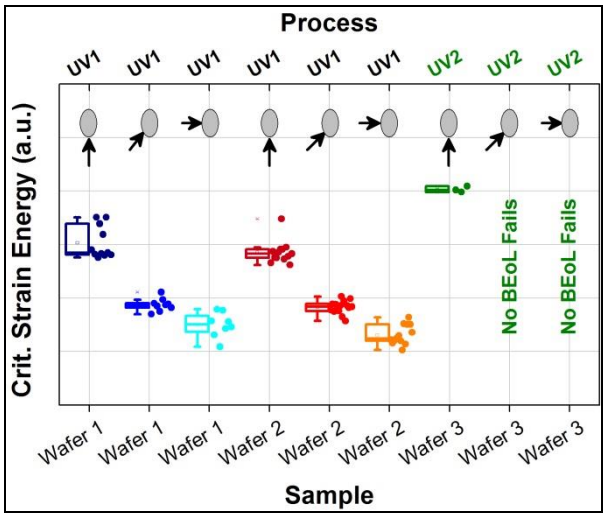

Fig. 15: Critical strain energies for BEoL failures induced by SPSTs on 3 wafers. The 45deg and 90deg tests on wafer 3 lead to different failure modes on top of the contact pads, i.e., no cracks were found inside the BEoL stack, indicating even higher BEoL strength.

Most interesting, the critical strain energy increases further for wafer 3 with UV2 process, as shown by a very few remaining BEoL crack events for 0deg. shear. All other tests on wafer 3 lead to fBEoL failure modes without any cracks in the BEoL stack, especially for 45deg. and 90deg. shear. That means, the BEoL layer stack of wafer 3 is mechanically stable under the conditions of the applied loading mode of the SPST, and the applied forces just lead to plastic deformation of the Cu Pillars and the aluminum pad or peeling off of the Cu Pillars from the pad.

Finally, dies with the improved BEoL process UV2 had been assembled and tested. A significant yield loss reduction had been observed as predicted by the shear test results on wafer level (Fig.16).

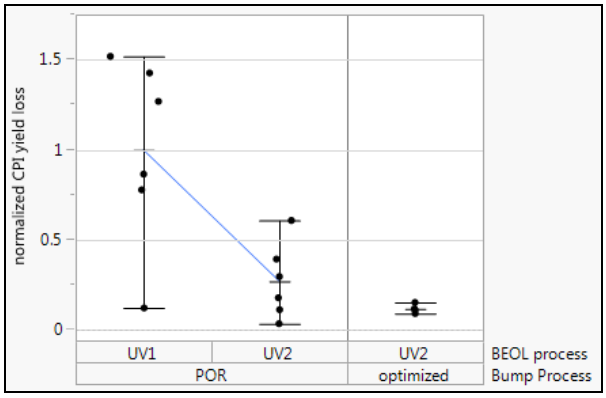

Fig. 16: Assembly yield loss with optimized BEoL and bump process parameters.

III. Conclusion

Modeling was used to predict how a change in the Cu Pillar geometry impacts the CPI failure rate. The modeling results are in close agreement with the experimental data, indicating that the models used here are well suited to predict process improvements to reduce the number of CPI related failures. The modeling and shear test results also predicted the impact of adjusting processing parameters in BEoL, such as UV correctly. The majority of process improvements described in the paper is implemented out to volume production.

Acknowledgment

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