ASSESSMENT AND CHARACTERIZATION OF STRESS INDUCED BY VIA-FIRST TSV TECHNOLOGY

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Abstract

Through Silicon Via (TSV) is a key enabling technology for 3D stacking. One of the main concerns regarding the TSV introduction inside the IC fabrication is the resulting stress build up in the silicon substrate that may induce warpage or expansion at the wafer level, strain and crystalline defects in the neighboring silicon of the TSV and finally can impact performances and reliability of the CMOS devices as well. Polysilicon, tungsten and copper are the three main conductors that are nowadays considered for the TSV fabrication. In a first part of this paper the different factors that contribute to the stress in these tree TSV types including the geometry, the materials and the process will be reviewed.

After bonding on a temporary carrier and thinning of the substrate to expose the via the stress built up during the fabrication of the TSV can be also revealed by the expansion of the silicon membrane.

Thermo-mechanical FEM simulations will be equally introduced and confronted to the experimental findings.

We also present some characterizations of silicon defects by chemical revelation around the TSV structures.

For characterization of the stress in TSV structures scale different techniques as EBSD, µRaman, XRD will be then presented.

Finally we conclude that with the optimization of some key processing steps, the stress induced in via-first technology may be acceptable for IC integration.

Keywords: TSV, via-first, stress, polysilicon, tungsten, copper, FEM simulation, physical characterization.

Introduction

As miniaturization of the CMOS components are becoming more and more difficult and costly new fields for improving the ICs performances are actively developed. One of the most promising ways is certainly the 3D integration of stacked chips. Through Silicon Vias (TSV) is most likely the solution to go to 3D device stacking [1-3]. Different integration schemes have been proposed, but no single solution has emerged as yet. The choice to make the TSVs before or during the devices fabrication (via-first approach) or after (via-last approach), the nature of the filling material (polysilicon, tungsten or copper); will mainly depend on the constraints of the final product. In the following of this paper we will focus on the different via-first TSVs technologies and particularly the stress effects related to its fabrication will be discussed. In the case of polysilicon via, TSVs are fabricated at the very beginning of the IC process flow, they imply high thermal budget but the thermo-mechanical properties of the materials used are close to the silicon ones. At the opposite via-mid TSVs are made with metal like tungsten and copper having higher Coefficient of Thermal Expansion (CTE) but requiring much lower thermal budget. Another important aspect related to the overall stress is the volume of materials used for a given resistance of the via and finally the density of interconnections that is related directly to the final application. Also the choice of the feature geometry is mainly dictated by the deposition techniques and has an impact on the surface of the TSV as well.

Stress can be monitored at different levels and with different techniques of characterization. First, at the wafer level the bow of the substrate is a very good indication of the stress build up during the successive steps of the process. During the backside processing stress can equally be evidenced by some dilation or

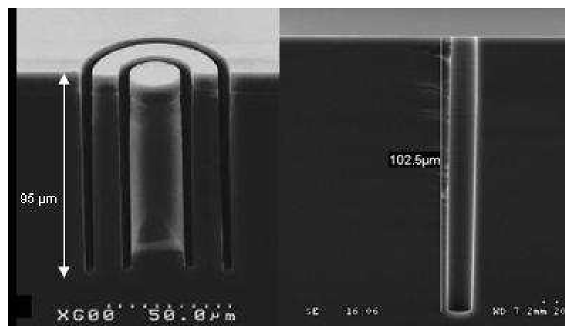
contraction of the thinned substrate. Then localized physical characterizations can be used at the TSV scale like chemical defect decoration, Electron Back-Scattered Diffraction (EBSD), X-Ray diffraction (XRD) and µRaman. Finally electrical testing can reveal also the effect of the stress either directly inside the TSV as well as in the neighboring CMOS devices [4].

Thermo-mechanical simulation analysis using Finite Element Modeling (FEM) is equally a powerful mean to assess stress behavior in the TSV structures and to establish design rules [5-6]. Some examples of such studies are also presented in this work.

Technology and design

A. Annular via technology for polysilicon and tungsten TSV

Annular shape vias [7-8], as well as narrow trenches array [9] have already been shown to be a good compromise to achieve low resistance while using relatively thin deposited films and are thus the more suitable designs for polysilicon and tungsten TSVs since these two materials can be deposited only with limited thickness due to high intrinsic stress and relatively low deposition rate. In this scheme, the resulting aspect ratio (AR) of the TSVs is higher than 20:1 for vias in the range of 100µm of depth (Fig. 1a). In spite of the above adapted geometry multi-step deposition are necessary to fill completely this kind of structures as well as intermediate etch back process to limit the stress build up resulting from the relative thick layer on top of the wafer.



a) 2 rings design used for poly and W b) cylindrical design for Copper

Figure 1: Illustrations of the TSV structures in Si substrate.

B. Copper via-mid technology

For copper via-mid technology the best geometry is the one with cylindrical holes (Fig. 1b) since the filling process is not much limited by the thickness of copper obtained by electroplating deposition. Inversely the process limitations are mostly resulting from the aspect ratio of the cavity that can be filled by this technique of deposition as well as for the barrier and seed layers that need to be firstly deposited.

Intensive work has been carried out to develop new electroplating hardware and chemistries capable of filling aspect ratio typically greater than 10:1 in particular with the introduction of specific additives to obtain a super-filling effect, also called bottom-up filling [10]. With this optimized process, holes of 10 µm of diameter and 100 µm of depth can be filled with no voids inside the copper. Meanwhile such structure represents a large volume of copper having a high CTE embedded inside the silicon substrate. Any thermal gradient that may be applied to the wafer during the TSV fabrication and after may lead to important stress concerns. However, since the electroplating deposition is made at ambient temperature the filling may not be a source of thermal stress. Thermal budget will come during the subsequent process steps including the copper annealing generally performed at relatively low temperature (150 °C) and moreover the interconnection thermal budget that is in the range of 400 °C for CVD dielectrics deposition.

C. TSV insulation

Since there is no temperature limitation for via-first TSV the best candidate for insulating the structure is thermal oxidation. Other deposited oxides can also be considered like High Temperature Oxidation (HTO) or also TEOS/Ozone Sub Atmospheric CVD (SACVD) oxide [11] followed by a high temperature annealing for densification of the layer and improving its electrical characteristics.

In the range of temperatures acceptable for mid-process technologies there are two available deposition techniques that gather the expected criteria of good film conformity and good electrical properties: (SACVD) or silane High Density Plasma CVD (HDP) [12]. The first oxide is preferred for aspect ratio such as 10:1 because of its very good step coverage in the range of 70 to 80%. In table 1 main physical data concerning these oxides have been listed.

Table 1: Physical data of TSV insulation materials.

Layer	*T°. of dep. (°C)*	*Stress As-deposited (MPa)*
Thermal oxide	1050	-320 (comp.)
HTO	730	-170 (comp.)
SACVD	480	+220 (tens.)

D. Metallization for via-first technologies

In table 2 we have summarized the main physical characteristics related to polysilicon, W and Cu via-first TSV. From these data some first assessment can

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already be drawn regarding the mechanical behavior of the TSV structure inside the silicon matrix.

Table 2: Poly, W and Cu physical characteristics

	Doped Polysilicon	Tungsten	Copper
Resistivity (µOhm.cm)	100[1]	12[1]	3
CTE (ppm.K^{-1})	2.7	4.6	17
Young modulus (GPa)	170	400	128
Deposition mode	CVD	CVD	ECD
Deposition temperature (°C)	1050[1]	440-470[1]	25
Maximum aspect ratio	30:1	30:1	12 :1
Intrinsic stress as-deposited (MPa)	220[1]	1400[1]	20

[1] *this work*

Polysilicon is very close to mono-crystalline silicon in term of CTE. Only non-elastic behavior links to crystallization changes can little affect the volume of the structure as well as the resultant stress inside the structure.

Tungsten CTE is much closer to silicon compared to copper. The main disadvantage of using tungsten as the filling conductive material is the high stress and modulus of the film that limits drastically the allowed deposited thickness and leads to delamination issues.

Then Cu in spite of a very high CTE has a low modulus and can sustain plastic deformation. Also it is applied at low temperature.

E. Test vehicles

For polysilicon and tungsten TSV technologies we used a specially designed test vehicles with annular TSV of different geometries; 2 rings and 3 rings with varying ring widths between 4 and 5 µm. Different test structures, like daisy chains of hundreds of TSVs are distributed repeatedly on the wafer resulting in homogeneous density of TSV at the wafer scale but with significant variation locally.

For polysilicon thick SOI substrate has been used for the requirement of the final product integration.

The wafers are finally tested electrically from the backside on a fully automatic tester to extract the TSV resistances and the isolation characteristics as well as the daisy chain yields.

For copper TSV technology the results presented in this work have been obtained using a dedicated design constituted by a photo-repeated array of 6 per 12 TSVs with diameter and spacing equal to 10 µm. This test pattern has been designed only for mechanical studies; no electrical measurement can be produced from it.

In this study, only TSVs are present on the test vehicles, there is no IC processing.

Results and discussions

A. Stress build up during TSV fabrication

During the fabrication of the TSV within the mechanical demonstrators the measurement of the wafer curvature is a very simple and efficient manner to monitor the stress build up related to the presence of the via structures. After each process steps the bow of the wafers is measured on a FLEXUS stress measurement equipment based on laser beam scattering method. The added layers on the top of the substrate are removed by etch back or CMP along the process flow such ways that only the TSV contribute to the wafer stress.

Polysilicon TSV technology

For the fabrication of the polysilicon TSVs the main process steps consist in the following flow detailed in previous work [13]: etching of the trenches inside the substrate by Deep RIE with Bosch process; side walls insulation by thermal oxidation or alternatively by High Temperature Oxide (HTO) deposition; filling of the trenches with highly phosphorous doped polysilicon with a sequence consisting of poly deposition plus Rapid Thermal Annealing (RTA) for further dopant activation plus partial etch back. This sequence is repeated three times to completely fill the trenches. Then, the removal of the polysilicon on the back side by dry etch back and of the front side by CMP are achieved.

Front side metallization is then realized using a classical tungsten contact plugs followed with aluminum lines level. Back side processing consists of bonding the substrate front side on a temporary silicon carrier using HT10.10^{TM} product from Brewer Science. This glue material has a glass transition (Tg) of 120 °C and a debonding temperature of 180 °C [14]. Backgrinding and CMP from the wafer back side are then performed to unveil the vias. Finally contact openings through a LTO deposition layer and RDL using Ti/Al metallization are formed.

Evolution of the wafer bow is presented in Fig 2. The original bow of the SOI wafers is already significant compared to bulk Si indicating a tensile stress resulting from the presence of the 2 µm BOX oxide and the 7 µm silicon active layer sandwich. Etching the 100 µm deep cavities through the SOI stack doesn't affect the wafer curvature. Note that in our design the surface of the TSV walls roughly represents the same surface than the wafer itself. Since the wafer front and back sides are protected by a nitride layer only the TSV walls surface are then oxidized. Since the trenches are still open the oxide layer on the sidewalls has only a weak contribution on the wafer strain.

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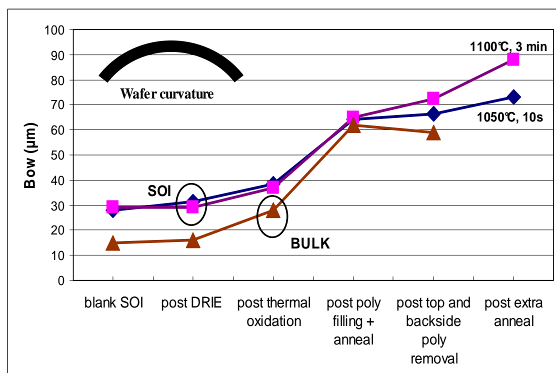

Figure 2: Wafer bow evolution during TSV fabrication (plotted in absolute value, bow is negative corresponding to a tensile stress) for SOI and bulk Si substrate.

With the filling of the trenches by the polysilicon material the bow increases significantly indicating an increase of the tensile stress in the substrate, note that the stress contribution of the top side poly layer is counterbalanced by the bottom side. In trenches polysilicon by itself may not induce a tensile stress since it is tensile as-deposited and become even more tensile after RTA. The increase of the strain is then mainly due to the oxide confined inside the filled cavity. Extra thermal budgets have been applied to simulate the subsequent fabrication of the CMOS devices. Higher temperature anneals lead to even more tensile stress due to higher thermal gradient.

HTO is an interesting alternative to thermal oxide in SOI stack for the TSV insulation because of its better coverage on the BOX side wall. It is deposited in a vertical furnace at 730 °C with Silane and N_2O gas mixture. As illustrated in Fig. 3, a split has been done using 1 µm of thermal oxide, a mix with 600 nm of thermal oxide plus 600 nm of HTO and only 1 µm of HTO.

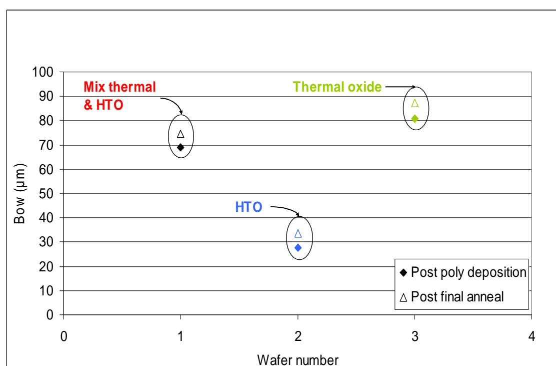

Figure 3: Wafer bow after TSV fabricated with different insulation oxides.

Replacing thermal oxide with HTO keeps the bow of the substrate near its value before TSV fabrication. In this experiment, the thickness of the HTO on the TSV walls is however divided by a factor of 2 compared to the thermal oxide case since the HTO step coverage is close to 50%. Moreover stress of the HTO film is also significantly lower than that of the thermal oxide as reported in Table 1. It is evident from these experiments that most of the stress inside the TSV comes from the thick side wall oxide thermal constraint that takes place in particular during the high temperature treatments applied after the poly deposition. In our process highly phosphorus doped polysilicon has only a small and favorable contribution to the overall wafer stress.

Tungsten TSV technology

Tungsten Chemical Vapor Deposited (CVD) as been widely utilized in VLSI CMOS technology for a long time, in particular for contact plugs to connect the silicided gates and S/D of the transistors to the BEOL interconnections. CVD tungsten is fully compatible with the middle end brick in terms of resistance to electromigration, metal diffusion, thermal budget, it has a relatively low resistivity (see table 2) and it is very conformal to fill the very narrow contact structures.

The main issue with the tungsten is the very high stress of the CVD deposition process particularly when a conformal layer is needed. In the TSV application the process requirements appear to be much more difficult than for the contact plugs because both the deposited thickness and the AR is one order of magnitude higher (respectively few microns of deposition and AR of 20:1 or higher). For instance, with our structures the space to be filled with W after deposition of the isolation oxide is equivalent to 2.5µm for the 4µm design and 3.8 µm for the 5µm design. It is not possible to deposit such a thick conformal tungsten layer at once otherwise the stress of the wafer will be too high. Different ways have been investigated in order to obtain a good filling of the structures while keeping the stress at an acceptable value [15]. In a first approach we used the deposition of a tungsten layer of 1 µm with very good film conformity, named Via-Fill. The stress of this film is of the order of 1.4 GPa tensile for 800 nm of deposition and 1 µm is the maximum value to keep the wafer bow acceptable for the subsequent process steps. With this film we found that the stress in the trenches was likely to be too high and end up with the delamination of the tungsten layer inside the structures (Fig. 4).

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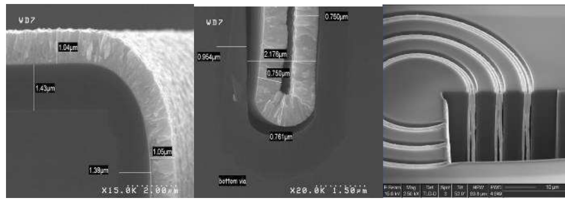

a) top deposition, b) bottom deposition, c)delamination
Figure 4: High conformal tungsten deposition SEM pictures.

Therefore a second process has been developed consisting in the deposition of a less stressed film with a slightly lower conformity. By this way the stress of the film is reduced down to 800 MPa for a film of 1.7µm while the film conformity is little degraded (-20% approximately).

In addition we used a multi steps deposition/etch back sequence to obtain a better filling of the trenches. With this process all the W is removed from the front side, stopping on the TiN layer meanwhile only few tens of nanometers are removed from the top trench walls and nothing in the bottom of the cavity.

In spite of this sequence the filling of the 4 µm trenches was not complete as depicted in Fig.5. In these conditions monitoring the wafer curvature during the trench filling does not allow to obtain a relevant indication about the stress build up at the wafer scale.

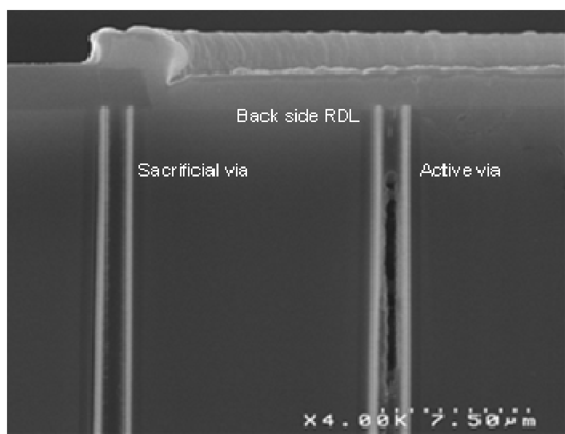

Figure 5: Bottom trench partially filled with CVD W.

Copper TSV technology

Copper is the metal of choice for low electrical resistances and it has been widely utilized in the damascene interconnections scheme during the last two decades. Electroplating deposition is well adapted for achieving tiny metal lines in structured dielectrics and continuous process improvements have been carried out to fill more and more aggressive aspect ratio structures. However in the damascene architecture the aspect ratio usually does not exceed 2:1 and the features to be filled are kept in the micrometer range. For TSV structures, because the substrate thickness can not be reduced too much for fragility reason the depth of the via is typically in the range of several tens of microns. As a consequence the diameter of the TSV can not be too small to keep an acceptable AR and thus the volume to be filled is also quite large. In our current via-mid technology the thickness of the thinned silicon is typically 100 µm and the diameter of the via is set at 10 µm to keep the aspect ratio at a maximum of 10:1.

For such aspect ratio usual deposition techniques like PVD deposition for copper diffusion barrier and seed layer as well as ECD deposition for copper filling are not adapted. In this work MOCVD have been used for the deposition of a 20 nm TiN barrier followed by copper seed layer of 150 nm. A full coverage of the cavities is obtained with this type of films.

For ECD deposition, we used the new solution provided by Applied Materials on the RAIDER-S^{TM} equipment equipped with RAPTOR chamber and the GENIII chemistry specifically developed for these types of applications. The principle of the filling mechanism is that the copper is growing essentially from the bottom of the structure avoiding the early closing of the upper part. As illustrated in the Fig 6 a complete filling of the deep holes is obtained with a limited over burden thickness on the top surface of the substrate of about 3 µm.

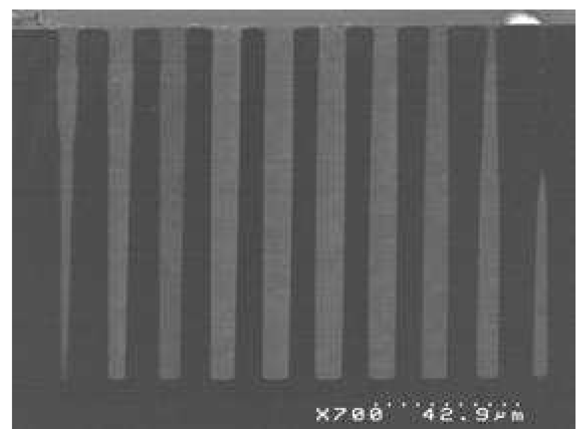

Figure 6: SEM cross section of 10x100 µm copper TSV array.

Like for polysilicon TSV the curvature of the silicon substrate has been monitored all along the fabrication of the copper structures as shown in Fig. 7. After Copper via filling only a very slight increase of the bow is observed indicating a very limited stress effect. When annealing the wafer at 400°C, 30 min an important increase of the bow can be observed. This increase is mainly due to the copper top layer yet

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present at the surface since it is well lowered after removing this layer with CMP.

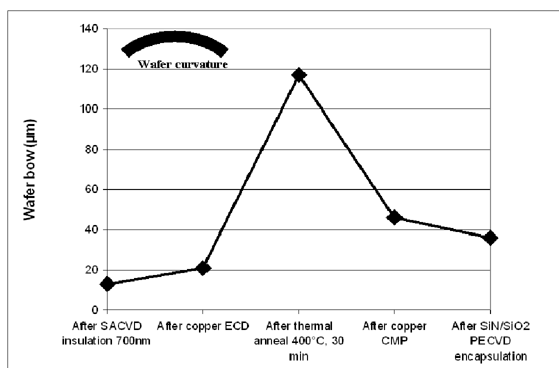
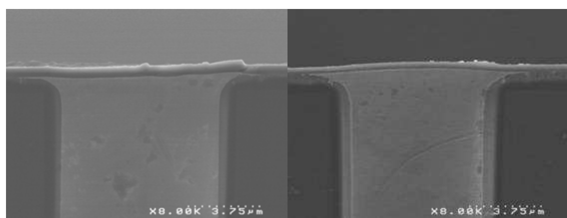


Figure 7: Wafer bow evolution during TSV fabrication (ploted in absolute value, bow is negative corresponding to a tensile stress).

The residual bow increase is yet significant indicating a residual stress originating from the TSV itself. During the annealing step copper is likely to undergo a plastic deformation that can explain that a residual stress is appearing in the structure during cooling.

This behavior can be also evidenced by the apparition of some copper extrusion at the top of the via as illustrated by the cross section of Fig. 8. However the importance of this effect is rather limited below 100 nm and can be controlled at the ECD process level as well.



a) No annealing b) 400°C, 30 min annealing

Figure 8: Copper extrusion with or without thermal treatment after CVD dielectrics encapsulation.

Plastic deformation and recrystallization behavior is much linked to the electroplating deposition process [16]. In addition to the filling capability properties new chemistries are also providing some major advantages in this field. This can be evidenced when comparing the extrusion height between an old formulation and the new one. Fig. 9 illustrates the results obtained in the case of the old chemistry showing that the extrusion can be as important as 3 to 4 µm and is also very dependant of the annealing temperature and not uniform across the wafer as well.

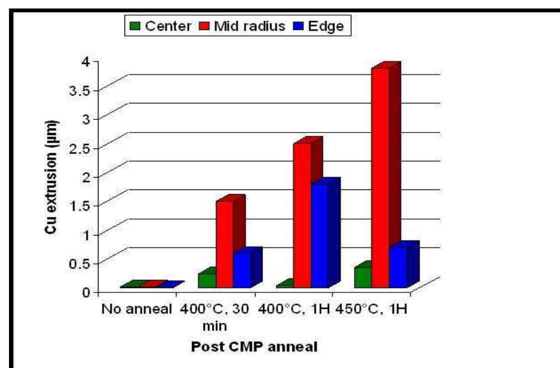


Figure 9: Cu extrusion after different anneals post CMP; with anneal pre CMP at 250°C and with old Cu ECD chemistry.

B. Stress release during back side processing

The stress accumulated in the upper part of the Si substrate by the fabrication of the TSV is likely to be released when the wafer in thinned during the back side processing. This effect may be limited by the use of a temporary carrier bonded to the substrate by a glue material. This phenomenon has been clearly evidenced in the case of the polysilicon TSV technology achieved in a SOI substrate as described in the following section. Inversely it was not observed with tungsten or copper TSV confirming that the stress is lower in these cases.

Polysilicon TSV technology

During the bonding operation the TSV wafer is flattened by the pressure inside the equipment and glued on the Si carrier. When unloaded the sandwich stays flat due to the symmetrical structure (Fig. 10c). When thinning the substrate (Fig. 10d) the stress inside the TSV strata induces the same curvature of the stack than it was inside the original SOI substrate of Fig. 10b meaning that the stress is thoroughly retained and transmitted through the glue to the Si carrier. During the LTO deposition at 240 °C (Fig. 10e), the temperature of the glue becomes much higher than its Tg leading to the relaxation of the stress inside the TSV strata exhibited by its expansion and by the flattening of the sandwich constituted by the silicon carrier and the TSV membrane.

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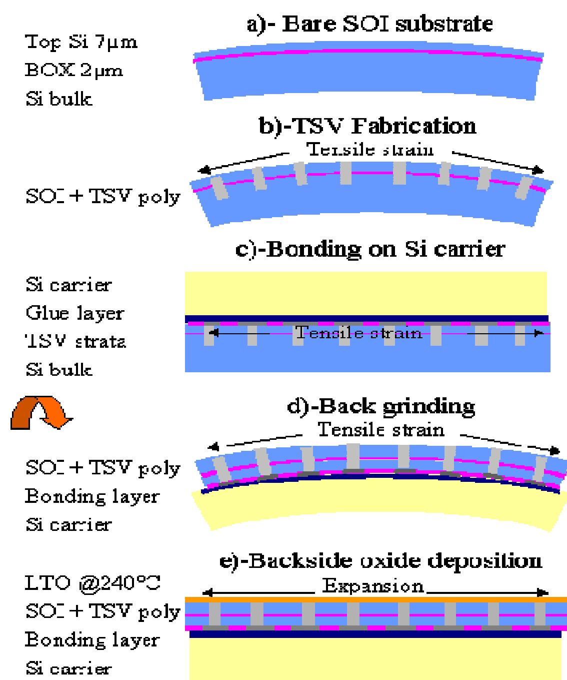


Figure 10: Behavior of the wafer bow during the TSV fabrication.

As illustrated in Fig. 11 the expansion is almost linear across the radius of the wafer starting from near 0 at the center and increasing to a maximum of 8 µm at the edge in the case of the 1050 °C TSV process thermal gradient. This value corresponds to 80 ppm of relative expansion on a 100 mm wafer radius. When no annealing is performed during the fabrication of the TSV (no RTA activation of the doped poly) the expansion is divided by a factor of two in the thinned TSV substrate corresponding to the 580 °C polysilicon deposition thermal gradient.

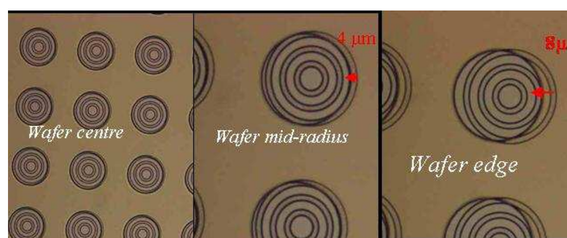


Figure 11: Back side contact misalignment with wafer expansion.

C. F.E.M. simulations

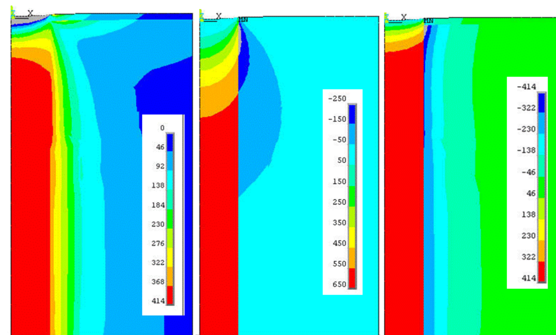
Polysilicon TSV technology

Taking into account the CTE of each material inside the trenches thermo-mechanical simulation is achieved to estimate the expansion of the TSV during the thermal cycle applied during the RTA anneals considering that the structure is in equilibrium (i.e. stress = 0) at the higher temperature. Relative dilatation of one TSV is obtained between a filled and an unfilled structure. We obtain respectively a differential radius variation of 0.019 µm for a via with 3 rings and 0.012 µm for a via with 2 rings for a temperature gradient of 1025 °C. Then we estimate the density of TSV on the wafer at 17 vias/mm^2.

Finally, by homogeneous extrapolation of the TSV cell displacements, we calculate the dilatation at the wafer scale. A dilatation of 10 µm on the radius is obtained and has to be compared to the 8 µm measured experimentally. When no RTA is applied, the maximum thermal gradient corresponds to the polysilicon deposition temperature at 580 °C and the expansion in then calculated at 6.4 µm, close to the experimental findings of 4 to 5 µm.

Copper TSV technology

FEM simulation has been performed using different TSV layouts with interconnect upper layer stack to assess the stress inside the structure and the extrusion issue as well. In this work an infinite 10 µm TSV spaced by 40 µm array is considered in axisymmetric model with fixed boundary conditions. In a first attempt thermo-mechanical copper behavior has been considered as pure elastic material with a stress free temperature at 250°C. At ambient temperature a maximum tensile stress value is obtained at 640 MPa for copper along the TSV side (longitudinal stress) with a contraction at the surface of 55 nm (Fig. 12).



a) radial stress b) axial stress c) azimutal stress

Figure 12: Copper TSV 10x80 µm stress simulation calculated at 20°C.

Since these very high values are not realistic and copper behavior can not be considered solely elastic between 20 °C and 400 °C a kinematic model as been implemented using yield and hardening modulus temperature dependence [17] (T is expressed in Kelvin).

$$Yield = 320\left(1 - \frac{T}{1000}\right)(MPa)$$

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$$Hardening = 75\left(1 - \frac{T}{1000}\right)(GPa)$$

Considering this time a stress free temperature at 20 °C and a thermal cycling temperature up to 400 °C we found that the maximum stress is in the range of 100 MPa tensile at 20 °C (Fig. 15).

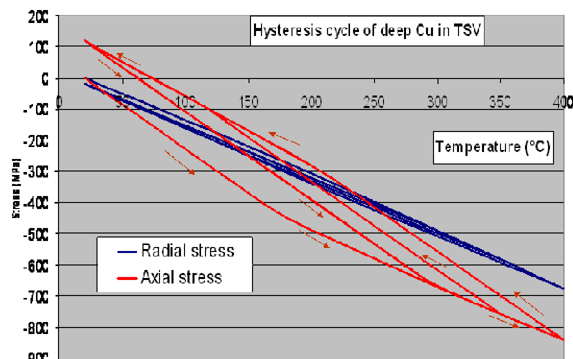

Figure 15: Copper TSV 10x80 µm stress simulation calculated at 20°C.

This value is possibly too low this time depending on the parameters used in the model. The displacement of the copper surface corresponds to an extrusion of about 15 nm which is better in accordance with the experimental findings.

D. Silicon defect recognition around TSV

Polysilicon TSV technology

The stress inside the silicon membrane may cause some crystalline defects like dislocations and slip lines in the silicon matrix that may be detrimental for the devices performances. After debonding the TSV membrane silicon defect analysis have been performed on cross sections inside and around the TSV followed by defects recognition with diluted HF plus Wright chemistry lapping [18]. In Fig.16, dislocations in the Si crystal are shown along the trench depth with a high density in the upper region and in particular near the BOX layer (picture 1 and 2). There are only few defects near the bottom of the vias (picture 5).

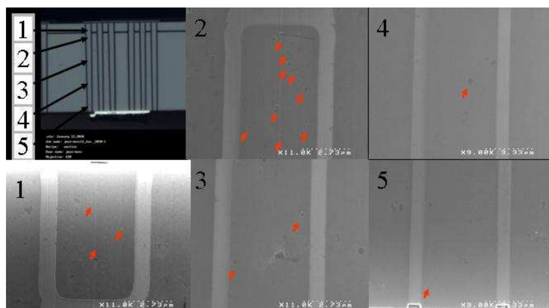

Figure 16: Si defects inside TSV trench after final debonding. Each red arrow indicates a single defect.

Looking at the upper region between two TSV the defects are localized only near the via walls at a maximum distance of less than 10µm as illustrated in Fig. 17 (picture 1 and 4). These observations provide a good indication that there will be no induced damage in the SOI stack by the poly TSV on the neighboring transistors even at a relatively short distance of less than 20 microns. Then most of the defects are localized inside the TSV rings near the BOX interface.

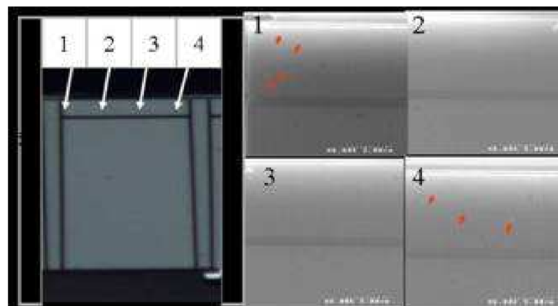

Figure 17: Si defect between two TSVs after final debonding..

Copper TSV technology

A sample with copper TSV has been also prepared for silicon defects recognition after filling and annealing at 400 °C, 1H (Fig. 18). No silicon defect was found at this stage of the integration confirming that the stress induced inside the silicon matrix by the copper TSV remains low compared to the yield of mono crystalline silicon.

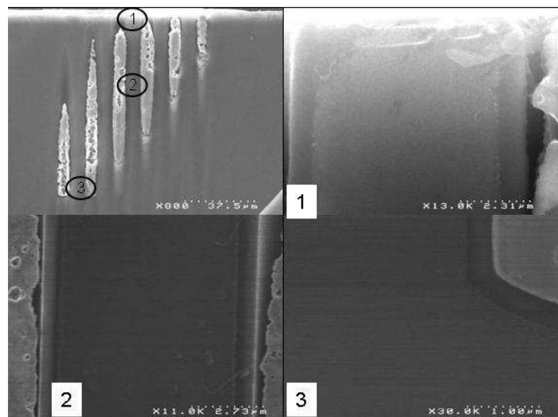

Figure 18: Si defects revelation of copper TSV structures after annealing at 400°C, 1H by Wright decoration.

E. Mechanical stress determination using micro-Raman spectroscopy

Micro-Raman spectroscopy is a non destructive analytical technique, based on the detection of photons scattered inelastically due to the interaction

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of the sample with a beam of monochromatic light. The frequency difference between photon scattered and photon excited provides information on the chemical nature of the molecule responsible for the broadcast. Materials whether in solid, liquid or gas states can be analyzed and information from a Raman spectrum are multiple (See Fig 19).

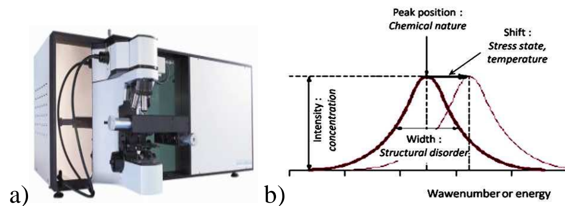

Figure 19: a) Raman spectrometer b) Qualitative and quantitative data provided by Raman analysis.

Micro-Raman spectrometry is used here to investigate the local mechanical stress generated in through-silicon via (TSV) when they are subject to flexural bending. Basically, maximal stress around TSV is investigated for various via design (diameter and pitch) [19].

Confocal micro-Raman spectrometer LabRAM HR (Horiba Jobin-Yvon) with CCD detector has been used at room temperature with HeNe laser of 633nm wavelength. A 1µm spot diameter with a power less than 1mW is used. A 2400 lines/mm grating was chosen in order to allow spectral resolution of about $0.1 cm^{-1}$.

For stress determination, a calibration procedure is made on 50µm thick bare silicon lamella. Raman reference peak position corresponding to stress-free silicon ($520.7 cm^{-1}$) is compared to the peak position of silicon under uniaxial mechanical bending (See eq. 1). The induced shift in frequency ($\Delta\omega$) is directly related to the generated stress (See eq. 2).

$$\sigma = \frac{e.E}{2.R} \quad (1)$$

$$\sigma = K.\Delta\omega \quad (2)$$

Where: e, E, R, K and $\Delta\omega$ are the silicon thickness (50µm), the Young's Modulus (130GPa), the applied curvature radius (25mm), the calibration coefficient and the frequency shift induced by mechanical stress respectively.

Calibration result shows that a K value of $435 MPa.cm^{-1}$ is obtained. After that, the stress developed in silicon around vias is recorded during in-situ mechanical loading, and compared with the spectral response of the reference. Fig 21 shows an example of Raman shift induced by mechanical stress.

Mechanical bending shows a Raman shift of $0.9 cm^{-1}$ and $0.3 cm^{-1}$ in transverse (points 1-2) and longitudinal (points 3-4) direction, respectively. Thus a stress of 391MPa is developed in the σ_{xx} component which is three time higher than the σ_{yy} one.

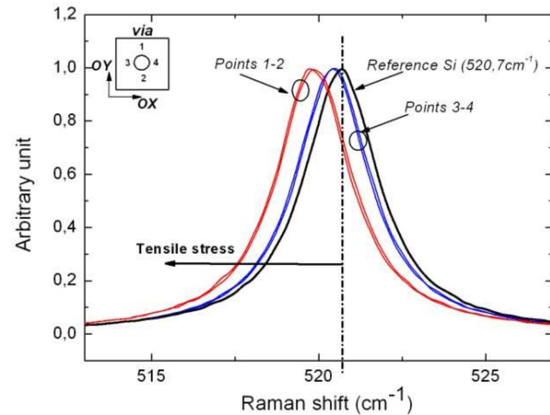

Figure 21: Raman spectrum obtained in different location around one via. The Si peak is fitted using Lorentzian. Inset shows the µRS measurement location.

Moreover, different via designs were investigated and experimental results are in good agreement with finite element analysis realized by ANSYS software (See fig 22). The ratio of via diameter to the distance between two vias shows a linear relation to the maximal σ_{xx} stress. In our case of study the corresponding ratio R is equal to 1 (D = 10 µm, pitch = 20 µm).

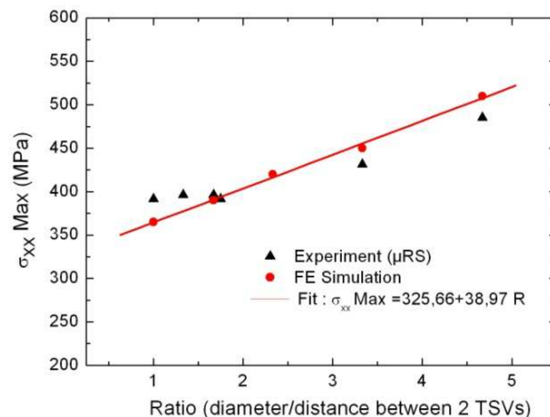

Figure 22: Effect of via diameter by the via-to-via spacing ratio on the generation of mechanical stress around TSVs, comparison between numerical model and µRS.

This study shows the use of micro-Raman spectroscopy as an accurate and non-destructive method to investigate the stress in materials and to allow for micro-packaging design.

F. X-ray stress measurement in TSV copper interconnects using the $\sin^2\psi$ method

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The $sin^2\psi$ method is usually applied to polycrystalline metals or metallic alloys to determine the macroscopic stress prevailing at the surface of the specimen and which extends over a length-scale much larger than the characteristic grain size. The stress generally varies with the depth from the free surface, therefore the values obtained from the X-ray measurement should be considered as an average corresponding to a mean penetration depth determined by the attenuation coefficient of the material and the diffraction angle 2θ of the selected Bragg reflection. The main assumption of the method is that the stress state is identical in each grain of the polycrystal. Its application to TSV islands embedded in single crystalline silicon presumes therefore that all copper TSVs are subjected to identical and constant stress state. The analyzed sample consisted in a cross section of an array of copper TSV after annealing at 400 °C during 30 minutes as depicted in the first part of this paper.

Measurements have been performed using the PANalytical – MRD diffractometer equipped with poly-capillary optics and a point detector with parallel plate collimator (PPC). The divergence of the PPC was 0.18°. The alignment of the optics was checked with a reference tungsten powder sample for which the difference in peak positions at ψ angles of -60°, 0° and 60° was less than 0.01°. For measurements the 220 Bragg reflection of copper was selected. The poly-capillary optics delivered a wide beam with cross-section of about 1 cm^2 illuminating many islands. The strain as a function of $sin^2\psi$ is shown in Fig. 23.

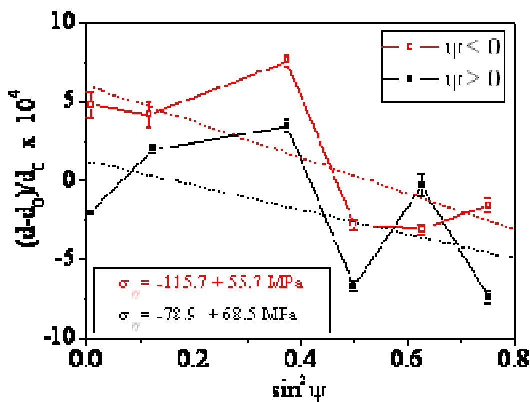

Figure 23: Average strain determined from the shift of the 220 peak as a function of tilt angle.

Its non-monotonous behavior indicates possible texture effects, i.e. an insufficient number of illuminated grains at different ψ angles. The fit of the data by a straight line indicates the existence of an average compressive in-plane stress component in the TSV. There is no real separation between strain data corresponding to positive and negative ψ angles. The stress determined from the two datasets leads to nearly identical values, however, the error of the evaluation is quite large exceeding 50%. Otherwise this result is consistent with the tensile stress previously obtained by FEM model and µRS. The inability of the applied global $\sin^2\psi$ technique to adequately describe the TVS system indicates that a different method capturing the stress in each single TVS would be more appropriate to characterize the system.

G. Measuring local stresses of copper TSV by EBSD

The Electron Back-Scattered Diffraction (EBSD) technique is nowadays a quasi-standard investigation tool for characterising microtextures (microstructural features in relation to their crystallographic nature and orientation). When coupled with EDX analysis, EBSD also provides powerful phase identification capabilities (see [20] for a recent overview). Since the pioneering work of Wilkinson and co-workers [21-22], EBSD is also increasingly used for elastic strain measurements at the local scale or plastic deformation analysis via GNDs characterisation. Figure 24 illustrates EBSD pattern formation: the incident electron beam probes the tilted sample (~70° tilt). Due to inelastic diffusion in the sample near-surface layer, a divergent internal source (S) is created, and diffraction of the back-scattered electron waves occurs (a process geometrically similar to Kossel cones). The diffracted signal is recorded onto a phosphor screen and forms an EBSD pattern where each pixel corresponds to the gnomonic projection of a crystal direction and the bands are associated to lattice planes.

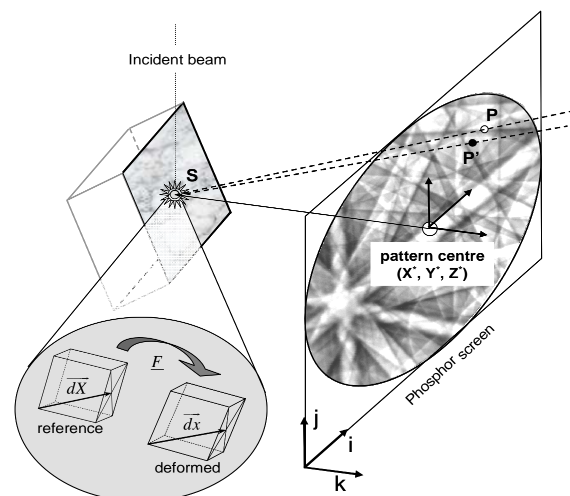

Figure 24: Schematic of EBSD pattern formation and the effect of a material deformation gradient tensor F displacing P to P' on the phosphor screen.

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The local elastic strain measurement relies on a comparison between a reference pattern and the current pattern by cross-correlation of a set of small Regions of Interest (ROI); the distortion field between the EBSPs, approximated by the discrete ROI shifts, is then used for the identification of the material deformation gradient tensor of the probed volume. In many cases, the strain state of the chosen reference is unknown, and HR-EBSD then measures the spatial variation of the deformation gradient tensor (see [23] for details). Using simulated patterns of elastically distorted crystals, Villert et al. [23] have shown that the applied deformation gradient tensor can be recovered with a typical accuracy of 10^{-4}. In the purely elastic regime the technique has also been experimentally validated for the case of SiGe epilayers and four-point bending of a silicon single crystal [24]. The spatial resolution of this technique is ~50nm, 150nm and 10nm for lateral, longitudinal and depth resolution respectively.

This technique has been applied to the same TSV cross-section prepared by ion milling as already depicted.

The cross section has been analysed by EBSD, using a Zeiss Supra 55VP FEG-SEM operated at 30kV with a probe current of ~2nA, and a chamber pressure of 10Pa. The EBSD analysis was carried out using an HKL system (now Oxford Instruments) composed of a NordlysII camera and the Channel5 software suite. Patterns were recorded at full resolution (1344x1024 pixels), with a mean integration time of about 2 sec per pattern. A linear scan of 150µm with a step size of 0.1µm was subsequently analysed with a reference point selected far away from the TSVs. The full stress tensor was obtained along the line scan (note: a plane stress condition can be safely assumed due to the shallow depth of the probed volume).

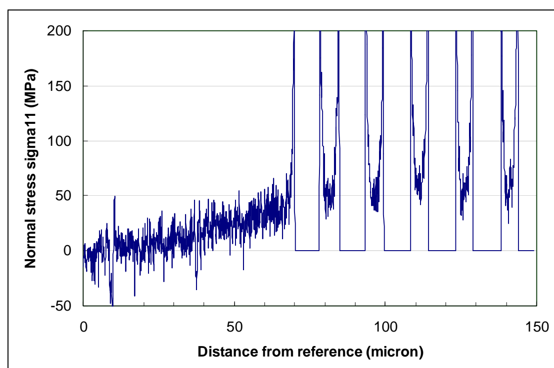

Figure 25: evolution of the normal stress □11 along the line scan.

Fig. 25 illustrates the variation of the horizontal normal stress profile when approaching the TSVs and in-between two copper vias. The traction stress is about 50 MPa in-betwwen the vias, but seems to rapidly increase in the vicinity of the copper, in agreement with mechanical models.

These first results demonstrate that HR-EBSD is able to reveal local stress distributions in TSVs.

Conclusions

Stress induced by the introduction of through silicon via structures inside device wafer is a key integration issue. These vertical interconnections are quite large compared to the device features and need to be relatively close to them for saving silicon surface and reducing the length of the interconnect lines. In this work we have detailed the main three via-first technologies based on doped polysilicon, tungsten and copper metallization and stress behavior has been highlighted in each case. A first general comment is that overall stress intensity is linked to a convolution of four main factors: the thermo mechanical mismatch between the materials of the TSV structure with respect to silicon, the intrinsic as-deposited stress of the TSV layers, the thermal gradients that are introduced after the via filling and then the volume of material used to achieve the required vertical interconnections. Each of the above mentioned technologies has pro and contra arguments in this perspective. However copper TSV offer the best compromise assuming that the size of the geometries can be reduced even further with improving the filling process capability.

Physical characterizations are keys to understand and monitor stress effects of the TSV in silicon wafers. Already existing techniques are being adapted and refined to address this field like XRD, EBSD or µRaman for example. However these techniques remain limited with respect to the spatial resolution when looking for local stress inside the TSV structure itself. Synchrotron beams penetrating into the bulk are expected to bring more insight into the local stress distribution. These physical analysis need to be also associated to accurate modeling of the structures, in particular with non-elastic behavior of the materials.

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