Mechanical Insertion and Reliability Testing of Thermal Interface Materials for Semiconductor Test and Burn-in Applications

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Abstract
Semiconductor test and burn-in requirements for thermal interface materials (TIMs) are challenging, with difficult mechanical reliability requirements that are not found in other types of applications for these materials. To demonstrate the ability of certain newly-developed TIMs to not only provide suitable thermal performance for the device under test and meet these mechanical requirements, a contact cycling test has been devised in three phases for evaluating TIM mechanical performance and durability.

Key words
Thermal interface material (TIM), testing, semiconductor test, burn-in.

I. Introduction

Many categories and types of thermal interface materials are manufactured, designed for a very wide range of different types of applications for semiconductor devices. Semiconductor test and burn-in applications represent what may be seen as the most challenging requirements for TIM performance and reliability, as these requirements include multiple insertions of the test head with TIM attached, to contact hundreds or thousands of semiconductor devices under test. Certain test procedures include relatively high temperature as well (up to 155°C) for burn-in and may also require that non-parallel contacting surfaces. These mechanical test requirements place significant challenges on the durability of the selected TIM, in addition to the normal thermal resistance, thickness, material type, and similar requirements. A mechanical cycling test program was devised to test a set of three recently-developed types

Table 1. Thermal /Mechanical Cycling Test Program Design

Program Phase	Purpose	Test Head Configuration*	Operating Temperature (°C)	Data Output
I	Baseline Values	Parallel	70 – 95	R_{th}** Thickness Change*** Cycle Count
II	Strike Angle	Upper Body: Strike Angle	70 – 95	R_{th}** Cycle Count
III	Strike Angle/Elevated Temperature	Upper Body: Strike Angle at Elevated Temperature	125	R_{th}** Cycle Count

*Notes: * Test head configuration and test system design per ASTM D 5470-17 thermal interface material testing methodology. ** Thermal resistance value is the principal thermal performance value for a TIM and uniform, stabilized test values for Rth and thickness indicate an appropriately stable test procedure. *** Thickness change data is intended to provide an indication of stable test cycling process.*

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of TIMs designed specifically for use in semiconductor test and burn-in, to generate much-needed information on reliability performance in difficult circumstances and number of contact cycles achieved. The intention for this test program is that all testing be conducted by an independent laboratory practiced in the design and manufacture of the required test stand, knowledgeable and experienced in thermal interface material testing, and experienced with reliability testing procedures.

II. TIM Requirements for Semiconductor Test

Many semiconductor manufacturers and semiconductor packaging companies perform an array of functional tests for wafers, singulated but unpackaged die, and packaged devices. Many of these test programs utilize various electrical performance tests for performance binning, as well as testing at elevated temperatures to stress and cull potential early device failures. The electrical performance testing and stress testing requires contacting each semiconductor device in a specialized test system with either an array of pin probes to establish electrical contact or, in a common test stand design, with a test head containing heating and cooling hardware, to apply rapid cooling and heating to the device under test (DUT). The following discussion applies to systems designed with this type of heated and cooled test head, normally a flat contact surface incorporating heaters and one or more thermoelectric modules or liquid cooling within the head. Contact with the DUT therefore requires the use of a TIM to establish intimate rapid heat transfer for the desired heating or cooling, as well as to maintain the semiconductor device at a specified maximum temperature [1, 2, 3].

In electronics thermal management generally, the typical application for a TIM requires the material selected to be placed once on a surface such as a heat sink or liquid cold plate or other metal component; this hardware is then assembled to the semiconductor package, completing the installation. The focus for material development is therefore on TIM thermal performance, the type of dispensing or assembly placement required, and the ability of the TIM to operate reliably once assembled over the expected product life without degradation. There is no requirement for repeated contact cycling. Only in the case of a component failure is there a recommended rework process that will include removal of the TIM, surface cleaning, and placement of a new TIM.

Directly contrary to these very typical application requirements, the TIM applied to a test head for a semiconductor test and burn-in system is expected to contact multiple devices in a specified procedure that is similar to a mechanical cycling test for the TIM. In high-volume semiconductor testing, the goal sought by semiconductor manufacturers is the ability to contact thousands of devices per twenty-four hour period with a single TIM applied to the test head. This is a very challenging requirement for a material that is designed to be compliant and yet provide excellent thermal performance, based on a design goal for a high percentage of surface wetting with minimum thickness. Given that devices under test may vary in size, shape, surface roughness and flatness – all of which the test system is designed to compensate for during operation – the TIM may be exposed to a "strike angle" if the gimbaled test head rotates to contact a smaller device. Such requirements for a strike angle contact exacerbate the challenging requirement for TIM durability. Further, this combination of conditions to which the TIM is exposed are worsened if testing is conducted at a higher ambient or test head temperature (i.e., up to 155°C) [4, 5]

Few thermal interface materials are capable of meeting such challenging requirements, given that the primary and typical application of a TIM is to a semiconductor device or to a thermal solution (heat sink, liquid cold plate, or similar) for a *single* application and the completion of the assembly. No traditional TIM is designed to meet a requirement for repeated contact, placement, and assembly between two surfaces.

A test program was developed, with assistance from a number of semiconductor test industry participants, in order to establish initial contact cycling durability results for several recently-developed TIMs. These metallic TIMs utilize several different design concepts, each intended to meet application requirements specified by one or more potential customers. Goals for the number of test cycles that a single TIM application may be required to meet range from a single contact for very high value devices to hundreds and thousands of device contacts for high volume, high through-put operations (such as test procedures for common microprocessors). Development of a TIM that is capable of reliably and repeatedly withstanding one to five thousand such cycles is challenging, as described above and as the TIM must also provide a target minimum thermal resistance value throughout the duration of use.

III. Requirements Determination

A test program was developed with assistance from engineers surveyed across an array of companies involved in semiconductor test and burn-in, including manufacturers of semiconductors, test equipment, test sockets, and burn-in array chambers.

Primary test criteria established were:

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a. Contact test pressure
b. Test temperature range (low to high)
c. Contact dwell time

The questionnaire used for this survey was conducted via email and telephone and in person; data was assembled and the averaged values shown in Table 1 were prepared based on these questionnaire results. Not all companies surveyed provided contact test pressure values, but there was sufficient data on all points to design the test program.

The test program was designed, based on these input values, to be conducted in three phases as shown in Table I. Data to be generated in Phase I would serve as baseline data, with parallel surfaces contacting in the same manner as would be found in standard thermal performance testing per ASTM D 5470-17, in a test stand designed to follow this industry standard test methodology. Phase I data would therefore represent a control for the subsequent phases.

Phases II and III were designed to mimic the test procedure requirements whereby a strike angle is implemented (Phase II), followed by increased temperature above the baseline value and combined with the strike angle (Phase III). The same test platform is to be used for all phases of this test program.

III. Test Platform

This test program was designed to be implemented using a recently-introduced commercial test platform, configured specifically to follow the requirements of the ASTM D 5470-17 thermal interface material testing methodology. The selected test stand, developed by Berliner Nanotest und Design GmbH (Berlin, Germany), utilizes servo motor control and internally-developed software that was originally designed to enable a variety of TIM test procedures to be undertaken, expanding beyond the requirements of the ASTM standard. This test platform, well known in the European Union and utilized for TIM testing by a variety of major electronics OEMs, has also been used previously for a range of TIM reliability and durability testing, including repeated cyclical compression and expansion of gap-filler materials [6]. Knowledge of the successful conclusion of these earlier reliability test programs was key to the selection of this specific test stand design. Automation of a mechanical cycling contact test, with recording of thermal performance values for each contact, as well as precise set points for contact pressure and test head temperature, with a specified dwell time for contact and for release, allowed this program to be conducted at reasonable cost without constant monitoring by a lab technician. The generation of thermal performance values in Phase I is intended to provide an additional control, whereby any excursion during testing would be immediately apparent in the thermal resistance data generated. Such data excursions could be due to tearing or failure of the TIM during the mechanical contact cycling; failure of a power supply, heater, or sensor; or similar. Thermal resistance curves generated therefore provide an additional control mechanism for the test program.

Figure 1.
ASTM D 5470-17 Test Platform



Table 2.
Thermal /Mechanical Cycling System Design

Property	Value
Test Platform	Berliner Nanotest TIMA6
Upper Reference Body (Heater Bar)	125°C
Lower Reference Body (Liquid Cold Plate)	75°C
Sample Temperature	95°C
Clamping Force Method	Servo Automated
Clamping Force Applied	500kPa (72PSI)
Temperature Measurement	In situ
Thickness Measurement Under Force Applied	In situ

Notes:
** Refer to text description for HSK patterning.*
*** Non-silicone dry-to-touch thermally conductive compound.*

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The selected test platform is shown in Figure 1. This is a standardized commercial test stand incorporating servo motors for precise test head movement and application of pressure for clamping force (in place of a pneumatic drive or manual control).

The configuration of test heads, temperature values, and pressure applied during each contact cycle are described in Table 2, using the standard test platform configuration and making use of the controls incorporated in the system. The test head alloy, flatness, and roughness were also specified, per normal TIM testing procedures.

IV. Materials Tested

Three recently-developed thermal interface materials were selected for this test program, for evaluation per the requirements determination (stated above). These three different forms of metallic TIMs were developed specifically to meet the challenging requirements identified for semiconductor test/burn-in applications. These materials are described in Table 3.

Each of the materials to be tested was developed as a metallic TIM using a different metal alloy and differing configuration, for specialized requirements. These material developments have been described previously [7], as have a small number of competing concepts [8]. The application of an aluminum cladding to one side of an indium flat foil is a development, for example, that provides an improved surface characteristic for rework and to prevent the possibility of leaving any material residue on the DUT, given the relatively soft tackiness of indium metal. While the aluminum cladding reduces the thermal performance of the TIM slightly, the result is a minimal difference and the handling and rework capability is improved significantly. The application of a patterning to an indium flat foil has also been demonstrated to improve thermal resistance and the ability to fill larger gaps between mating surfaces. Use of a thin aluminum foil with a non-silicone dry thermal compound applied to one surface only accomplishes an improvement in thermal resistance, without a soft compound contacting the DUT and leaving residue on the DUT surface, a principal requirement.

Table 3.
Thermal Interface Materials Tested

Graph Key	Description
CLAD	Indium (99.99%) flat foil, clad one side only with aluminum (0.0005" thick)
CLAD HSK	Indium (99.99%) foil, clad one side only with aluminum (0.0005" thick), HSK pattern applied*
HSMF-OS	Aluminum foil (0.002" thick), coated one side only with dry thermal compound**

V. Test Program Results

A goal set for this test program was to determine which, if any, of these three development materials could demonstrate successful results through each test program phase, to 1,000 cycles.

Given the wide range of semiconductor testing undertaken globally by semiconductor manufacturers and package assembly companies (OSATs), selecting a target cycle count is understood to be relatively arbitrary. A demanding set of test parameters are needed, to determine usefulness of these new TIMs. The parameters and goals selected are based on a common statement from OSATs and semiconductor manufacturers that a TIM that is capable of withstanding contact cycling of 1,000 DUTs would be viewed as a successful material development. Successful test results with implementation of a strike angle and elevated temperatures (i.e., 105°C to 155°C) would be highly desirable, to improve yield and speeds in semiconductor test and burn-in, with minimized testing costs [9].

Phase I testing has been completed per plan and all three materials selected for testing successfully passed the 1,000-cycle goal, before each test was shut down. The test results as shown in Figure 2 (below) provide thermal resistance over number of cycles completed (and time); as is commonly seen with TIMs of these types, the thermal resistance value improves with pressure and time.

A control measurement, thickness under test, is shown in Figure 3 (below); one of the values measured is thickness of the TIM under the specified pressure applied during each test. The figure demonstrates thickness achieved (Y-axis) under test versus cycle count and time. Reduction in thickness under pressure applied (72PSI for each cycle) for TIMs of these types also follows what is expected; the dwell time for each contact was set to one minute. The relative compressibility of each material and degree of surface wetting achieved is important. While thermal resistance is the critical value for performance of a TIM, achieving a relatively *very thin* material under compression is one of the principal determinants of lower (improved) thermal resistance.

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The next two planned test phases in this program are now underway. These phases are designed to further stress the TIM, applying a strike angle and higher temperature operation.

Based on a request from a major semiconductor manufacturer, an additional phase has been inserted into this program. This additional phase required testing in the Phase I test configuration to a new goal of 5,000 cycles. One material was selected for testing to this new goal, the material labeled as "HSMF-OS" and manufactured with an aluminum foil carrier (50µ thickness) coated on one side only with a non-silicone thermal compound. This TIM is designed to have the surface bearing the thermal compound coating applied to the test head; the compound has sufficient light tackiness to adhere to the test head prior to initiation of testing, without any fastener or pressure-sensitive adhesive required. This "HSMF-OS" TIM was tested and passed 5,000 cycles, the newly-established goal. The test parameters described in the initial Phase I test program were followed for this test.

VI. Conclusion

Testing of semiconductors (both bare die and packaged) to determine early failures and for the purpose of bin sorting ("binning" by frequency) is conducted in specialized test systems, using a range of different testing parameters. These test parameters include rapid cyclical contact testing, in some cases with very challenging characteristics such as a contact "strike angle" and elevated temperatures applied; certain manufacturers have requirements for test equipment and TIMs to be able to adapt to high-volume sequential testing of a variety of different package shapes and dimensions. A TIM is applied to the test head during this testing, resulting in a mechanically demanding requirement for new thermal materials capable of withstanding multiple repeated cycling of a single TIM, in contact with devices under test.

A test program has been designed based on a survey of industry manufacturers and current requirements. Three phases were initially developed for this test program, with increasingly demanding parameters; an additional phase was added based on a customer request. To date, two of the resulting four phases have been successfully concluded with excellent, reportable results documented herein, using an industry-standard test methodology that would allow replication of these tests elsewhere. The final two phases of this test program are underway as of this writing (and results are expected in time for final presentation).

The test program tested three different types of metallic TIMs developed specifically to address challenging mechanical and thermal requirements from semiconductor industry manufacturers, including semiconductor manufacturers and OSATs.

VII. References

[1] Additional information regarding the design of semiconductor test and burn-in test heads, sockets, test parameters, and similar, can be found in existing literature.
[2] P. Tadayon, Intel Corporation, "Thermal Challenges During Microprocessor Testing", Intel Technology Journal, Q3, 2000, pp. 1-8.
[3] F.S. Boatright, Delta Design, "An Overview of Applied Passive Thermal Control Technology for Integrated Circuit Test", Burn-In and Test Socket Workshop 2006, Mesa AZ USA, March 12-15, 2006.
[4] C. Lopez, Antares Advanced Test Technologies, "Semiconductor Industry Thermal Issues" (panel discussion, host presentation), Burn-In and Test Socket Workshop 2007, Mesa Az USA.
[5] J.A. Sanchez, Intel Corporation, "Challenges of Thermal Interface Materials in Test of IC Packages", IMAPS Advanced Technology Workshop on Thermal Management 2013, Los Gatos CA USA, November 5-7, 2013.
[6] "TIMA™ – Thermal Interface Material Analyzer", Berliner Nanotest und Design GmbH, www.nanotest.eu.
[7] R. Hunadi, "Specialized Metallic TIMs for Non-Flat Surfaces and Burn-in/Test Applications", IMAPS Advanced Technology Workshop on Thermal Management 2016, Los Gatos CA USA, October 24-26, 2016.
[8] C. Green, L. Prinzi, B. Cola, "Carbon Nanotube Polymer Composites as High Performance TIMs for Burn-in and Test Applications", Burn-in and Test Socket Workshop 2016, Mesa AZ USA, March 6-9, 2016.
[9] D. Saums, T. Jensen, R. Hunadi, C. Gowans, M. Abo Ras, "Development of a Mechanical Insertion and Reliability Testing Program for TIMs for Semiconductor Test and Burn-in Applications", IMAPS France 13th European Micropackaging and Thermal Management Workshop, January 31-February 2, 2018.

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Figure 2.
TIM Contact Reliability Test Results: Thermal Resistance vs. Contact Cycling

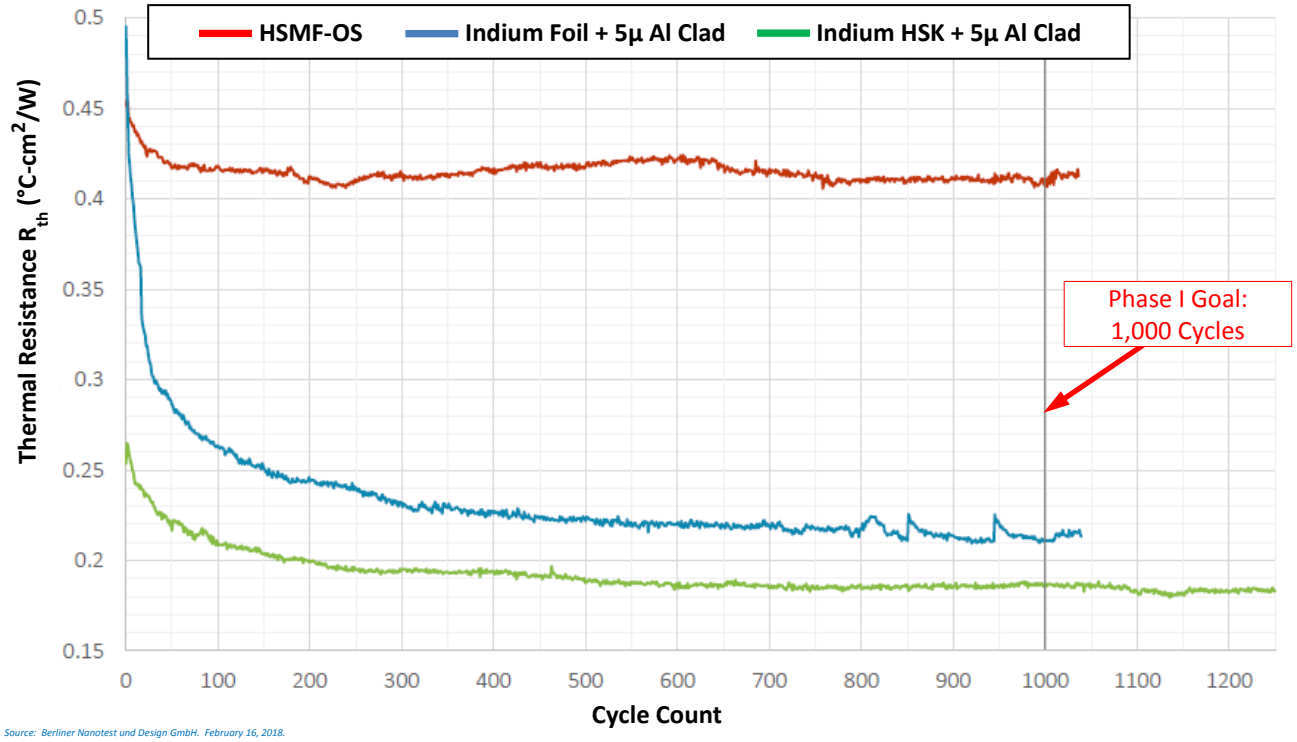
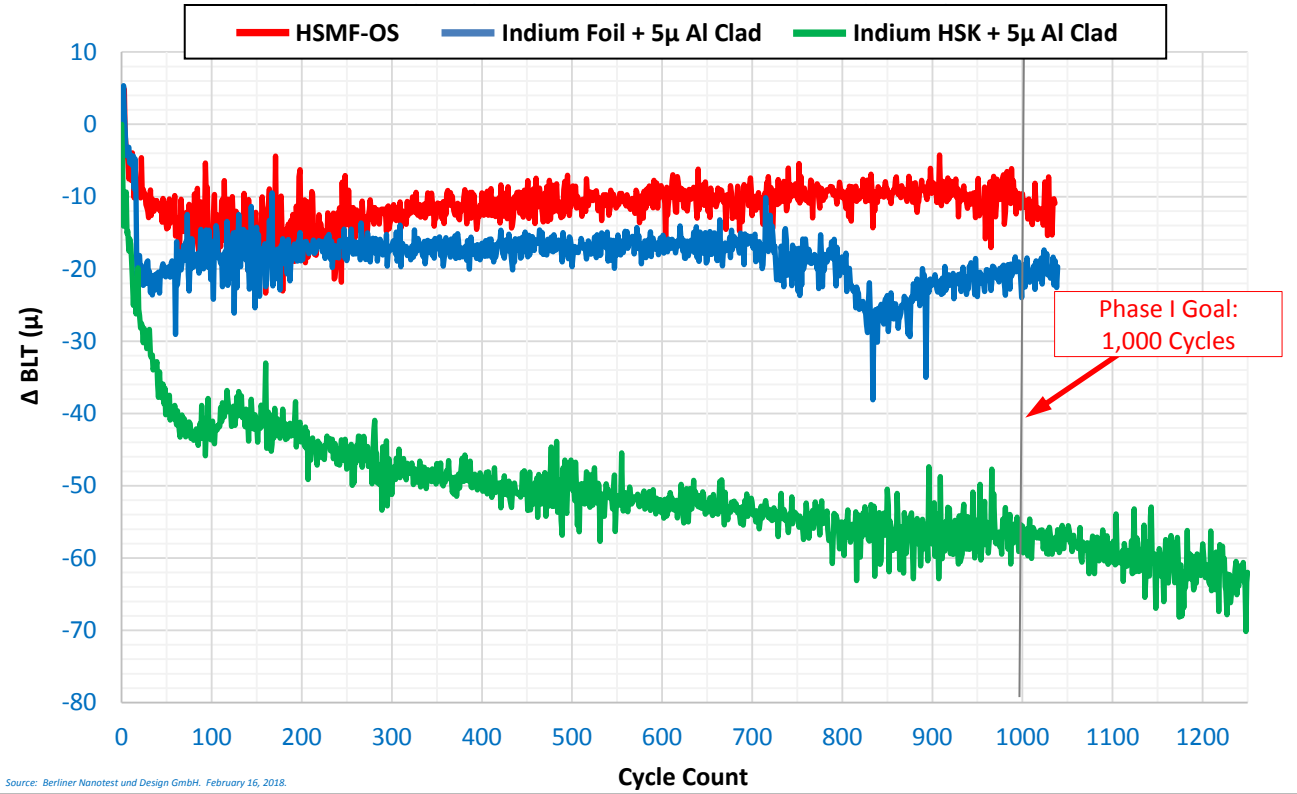


Figure 3.
TIM Contact Reliability Test Results: Thermal Resistance vs. Contact Cycling



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