Through-Silicon-Via (TSV) for silicon package: "via-bridge" approach

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Abstract

We present in this paper an alternative Through-Silicon-Via approach that can meet the new requirements of Si package. In this wafer level packaging scheme, a thick silicon interposer (200 to 300µm) is directly reported on a PCB. In 200mm Si wafers, we made a two steps TSV composed of two vias: a top via and a bottom via. The top via is etched with DRIE (diameter 60µm, depth 180 µm, Aspect Ratio = AR>3), and insulated with high temperature dielectric. After dry film lithography, the TSV is partially plated with Cu limiting the process costs (short plating time, no CMP) and the stress inside the TSV. After temporary carrier bonding, the wafer is backgrinded so that 15µm remains below the bottom of the main TSV. Backside lithography and DRIE process create the bottom via (four different diameters: 10-20-30 and 40µm) to contact main TSV. A final backside Cu plating of the opening completed the process. This via bridges the gap between via-last (AR<2) and via-middle (AR>7) and combines high temperature process from via-middle and low-cost processing from via-last. The mechanical simulations show that this "TSV bridge" has reduced residual stresses inside the TSV. Our electrical measurements exhibit an average single TSV resistance below 10mOhms with excellent yield (~95% on Kelvin and 82 TSV chains), and low contact resistances ($4.7x10^{-9}$ Ω.cm^2) extrapolated on 4 different contact diameters. This 200µm deep TSV seems therefore very promising for low-cost thick interposer applications.

Key words: TSV bridge, silicon interposer, silicon package, 3D integration, packaging

Silicon package concept

In the last ten years, 3D integration has led to an extraordinary breakthrough in the microelectronic packaging in terms of dimension reduction and performance. The silicon interposer became a smart way to bridge the gap between the advanced chips (node below 40nm) with the outer world package [1]. Si interposer ensures a good thermal matching with respect to the CTE of the reported dies, and benefits from high density wiring capability [2]. The key technologies are fine pitch interconnections and the vertical connection, the Through-Silicon-Vias (TSV). They allow connecting multiple heterogeneous dies together on a same silicon platform opening new devices possibilities. The silicon interposer is usually reported on a standard package like BGA, with bumps or large Cu pillars. A final passivation at BGA level ends up the packaging of the module as represented in Figure 1.

In an ultimate integration packaging scheme, Si interposer will be soon directly reported on the PCB in a Direct-Chip-Attach (DCA) process, thus forming a "silicon package". This will save the extra cost due to the BGA, and the individual packaging passivation. The silicon acts as the package itself, which can be process at the very last stage at wafer level. This offers even more flexibility in terms of heterogeneous integration. The concept of Si package is described in Figure 2.

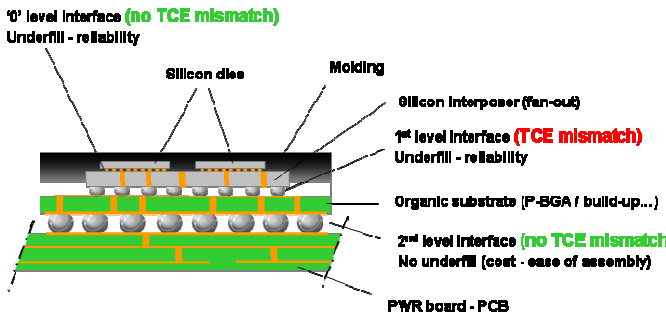


Figure 1: Packaging assembly with Si interposer

Of course, this implies some constraints on the si interposer. The first challenge is to manage the stress due to the CTE mismatch between the silicon (2.6 ppm/°C) and the PCB (~18°C/ppm). The 2nd level interconnection to the PCB board must be compliant with the elongation mismatch between organic and silicon. The pads finishing must be adapted to the solder balls. Several options inspired from fan-in packaging like double polymer cushion-layer help to release the stress. The second challenge to manage is the total robustness of the package. Classical thin silicon below 100µm would be

too fragile to withstand the reliability tests such as thermal cycling, drop tests, high temperature storage, etc…

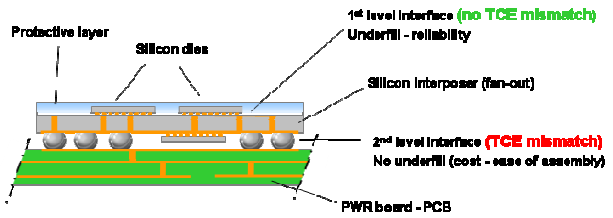


Figure 2: Packaging assembly of Si package

Very likely, the silicon thickness should be between 200 and 300µm to withstand thin wafer handling, front side chips passivation molding, wafer balling and to pass reliability tests. However, the conventional via-middle and the via-last integration scenarios [3] for Through-Silicon-Vias (TSV) could not address this thickness range. Indeed, theses vias can hardly go beyond 200µm depth [4],[5]. Some deeper vias have been already demonstrated as in **Erreur ! Source du renvoi introuvable.**, but with some costly process flow, long filling time and thus non industrial process. As a matter of fact, there is a need for vias for thicker interposer. This is obvious on Figure 3 that deep vias (deeper than 200µm) with medium or aggressive diameter have not been addressed so far.

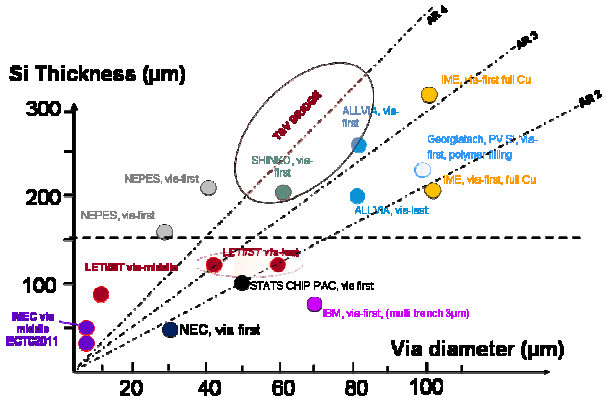


Figure 3. Benchmark of different TSV already published (firs, middle or last) from different groups with respect to the Si thickness and via diameter.

Therefore, we believe there is still some room for a new type of TSV. However, this must remain low-cost in order to remain cost-effective in the whole packaging scheme.

TSV bridge and mechanical simulations

In this work, we have developed and fabricated a new type of TSV. The idea is to benefit from the advantage of both via-last and via-middle technologies. A two steps process via uses the high conformality of the via-middle TSV for insulation and cu-filling to increase the moderate aspect ratio (<2) of the via-last TSV up to 4 to 5. Therefore, standard diameters of 50-60µm will lead to thicknesses range of 200-300µm. This TSV concept is named "TSV bridge" as it bridges the gap between the gap between via-last and via-middle. Figure 4 describes the TSV bridge in a Si interposer. It is composed of a top vis, fabricated from the front side coupled with a via bottom, fabricated from the back side of the interposer. If the Si interposer requires some metal routing level, the top via is made after the RDL line, etching through the top layers, as already demonstrated in [6] and [8] for example. The two via at top and bottom are filled with electroplating deposited copper (ECD) in the step than the routing layers (RDL), respectively.

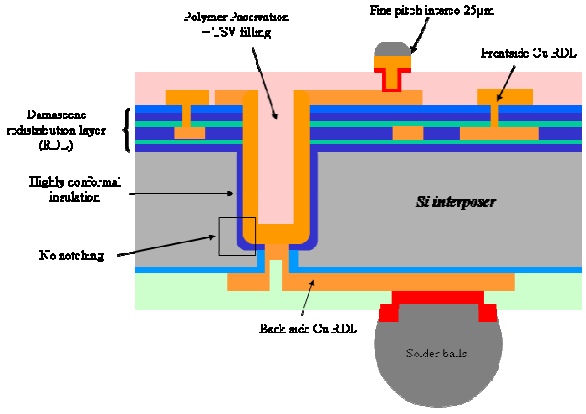


Figure 4: TSV bridge principle in a Si package concept with top and bottom vias

The top via benefits from high temperature deposition of back-end technology (400°C). Therefore, conformal deposition for insulation is available with technique like PECVD. In addition, the via etching stops into Si bulk substrate. The bottom corner of the via is round and smooth, on contrary of TSV last which induces notching. The seed layer deposition process is greatly improved leading to much better conformal deposition of the bottom. In order to limit processing cost and internal stress, the TSV is partially filled with electrolytic deposited (ECD) copper inside dry-film defined pattern. For most of the applications of the Si package, a few µm lining is sufficient in terms of resistance. Complete filled vias implies specific and expensive ECD chemistry solution, and a Chemical-Mechanical-Polishing (CMP) step is required to remove the overburden on top of the wafer. CMP is one on the most expensive step in microelectronic processing since the process is single wafer, long and uses expensive chemistry. Skipping the CMP step allows to keep the TSV bridge low cost compared to TSV middle technology.

The partial cu filling reduces the internal stress inside the TSV. Indeed, the Cu CTE (17 ppm/°C) is much higher than the one of silicon. It has been already demonstrated that in via-last, the reliability failure occurs at the junction between the via and the bottom metal pad, because of the significant stress of the Cu inside the TSV during thermal cycling [9]. In the TSV bridge, the mechanical stresses do not directly apply against the electrical connection between the top and bottom vias, but on the vertical and horizontal wall of silicon with oxide. This has been simulated with Ansys software, and the induced stresses after cycling from 200°C to 25°C are displayed on Figure

5. There is a smooth gradient of the stress inside the via, but not in the critical center of the via where the contact is done from the backside. The maximum stress is located outside the TSV. This is a promising result for reliability tests of TSV.

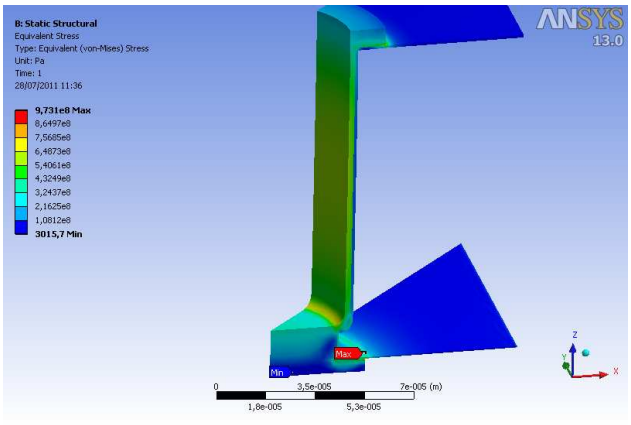


Figure 5: Simulation of mechanical van Mises stress in an 1/8th TSV bridge. 200µm deep TSV, diameter 60µm

In the next section, we detail the process flow and the challenge of the TSV bridge.

Process flow description

We describe in this section the process we use to fabricate the TSV bridge. We used standard 200mm monitor silicon wafer and CEA LETI MEMS200 mm clean room facilities. The Figure 6, Figure 7 and Figure 9 illustrate the process flow. The via_top diameter is 60µm, and the depth is chosen 180µm, leading to aspect ratio 3 One can easily extend this depth up to 300µm (AR=5) without any change in process flow. Step a) consists in Deep Reactive Ion Etching (DRIE) with the Bosch process to get straight via walls. The insulation of the via is performed with 500nm of SiO_2 SaCVD at 400°C with a conformal deposition better than 40%. Step b) is the seed layer deposition to allow electroplating. We use Ti(400nm)/Cu(1µm) from standard PVD completed by 200nm of Cu CVD to ensure a good electrical contact. In real industrial process flow, the seed layer can be deposited easily in modern ionized PVD tool, in aspect ratio up to 7 to 8. Therefore, seed layer is no longer a limitation with the via bridge process. The step c) consist in via filling. We use a dry film resist MX5015 from DuPont to define the plating area for the RDL. The partial via filling is done with standard plating chemistry with pulse current of 9mA/cm2. The Cu RDL is 7µm thick. Step d) is optional and consists of a passivation of the top surface with a polymer. Depending of the recipe and the material, we can fill partially the via_top with the polymer as described in [9]. We have tested here 2 configurations: no passivation and Asahi ALX 2010, 7µm spin coated and baked.

Once the front side is completed, the wafer is temporarily bonded in step e) onto a glass carrier with commercial HT1010™ bonding glue like described in [10]. Since there are unfilled vias on the front side, the polymer bonding had to be adapted in a vacuum bonding process. The wafer thinning follows in step f) by conventional coarse and fine grinding. As it can be seen on SEM cross-sections of Figure 8, the grinding stopped at 15 µm from the bottom of TSV_top. The final thickness of the interposer is controlled within +/-2µm with a good reproducibility.

Figure 9 describes the end of the process. First, the step g) pattern with a front –to-back alignement lithography the via bottom.

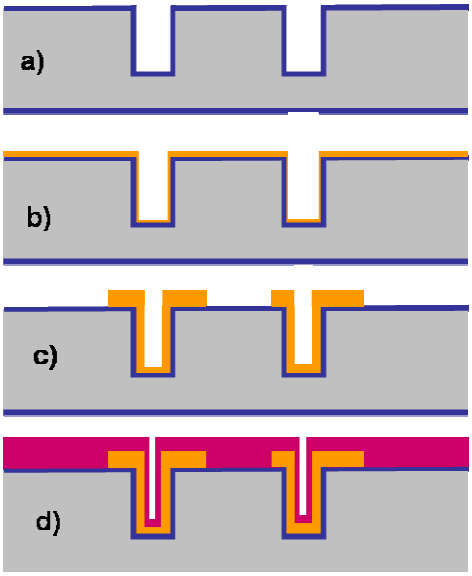


Figure 6: Front side process flow

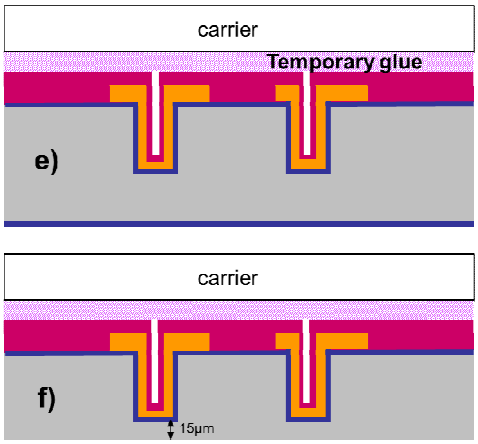


Figure 7: bonding and thinning steps

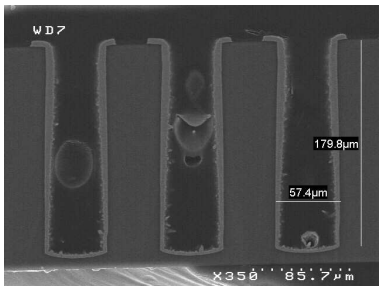


Figure 8: TSV_top after backgrinding until 15µm at bottom of the TSV (bubbles inside TSV are artefacts from cross-section preparation)

They are then DRIE etched from the backside until it reaches the via_top. The etch selectivity is good since the SaCVD SiO2 insulation layer acts as a stop layer. Four different diameters have been used for via_bot: 10µm, 20µm, 30µm and 40µm on different dies from the wafer. The goal is to assess the contact resistance versus the contact area between the via_top and via_bot as well as the process window for backside opening.

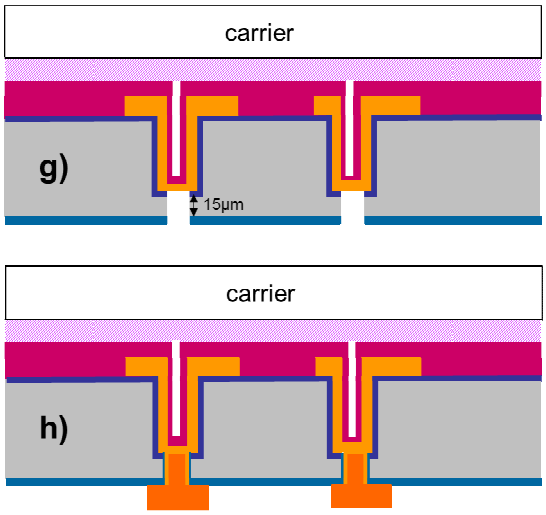


Figure 9: backside opening and electrical contact

Then, 500nm SiO2 low temperature (150°C) insulation is performed with a PeCVD on the backside. A final anisotropic etchback process is used to remove the deposited SiO2 in the contact area. A seed layer (Ti/Cu) is deposited and the via bottom filling is performed identically to via top, with dry film resist Cu electroplating (5µm ECD cu, 18mA/cm2), stripping and seed layer removal. The final stage is summarized in step h). Figure 10 shows optical pictures of the final backside RDL with the 4 different diameter of via bottom.

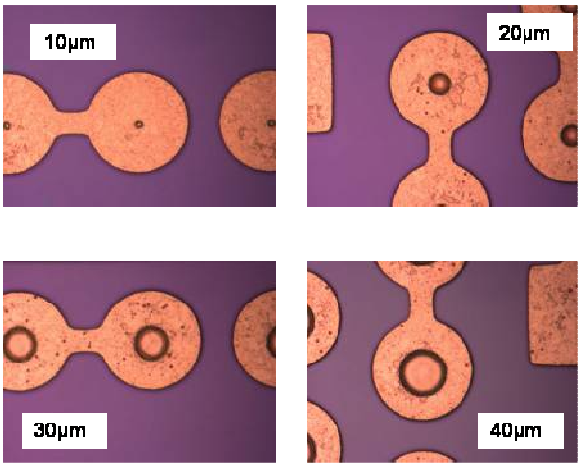


Figure 10: Four different diameters for TSV_bot: 10-20-30 and 40 µm, filled with copper

TSV bridge SEM inspections

Figure 11 shows a global cross-section of final TSV bridge daisy chains for 40µm via bottom. Figure 12 gives more details on the TSV structure. A partial Cu filling of 2.5µm is observed all along the TSV bridge. This corresponds to a 36% conformal filling compared to the 7µm deposited on top. The rough surface of the Cu comes from non ECD plating recipe, which can be optimized. No voids are detected on both via top and via bottom. The little delamination observed is thought to be issued from cross-section preparation.

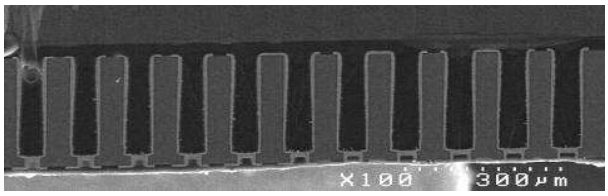
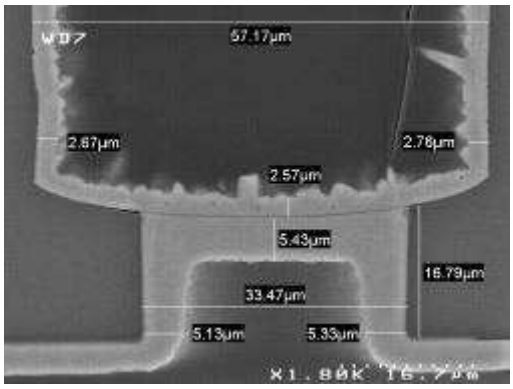
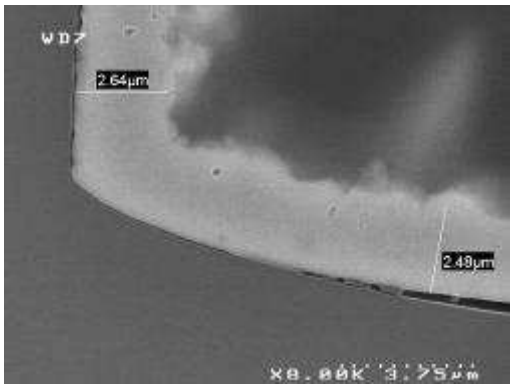


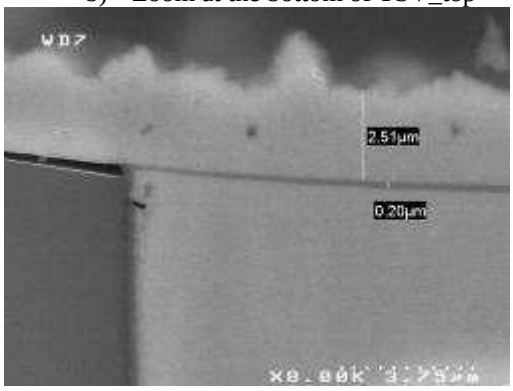
Figure 11: Global view of TSV bridge daisy chains



a) Contact between TSV_top and TSV_bot



b) Zoom at the bottom of TSV_top



c) Zoom at the junction of via_top and via_bot

Figure 12 SEM cross-sections details of the TSV bridge a), b) and c)

On Figure 12 c), one can see the good contact between the via bottom and via top. The dark line between the two vias is the two Ti seed layers from both vias, estimated at 200nm thick. For the smaller diameters 20µm and 30µm, similar results are observed. For the 10µm diameter, the via bottom is completely filled with cu.

Electrical test

Electrical tests have been performed on the wafer. The dies layout with respect to the via bottom diameter is reported on Figure 13. The wafer has been divided in four quarters.

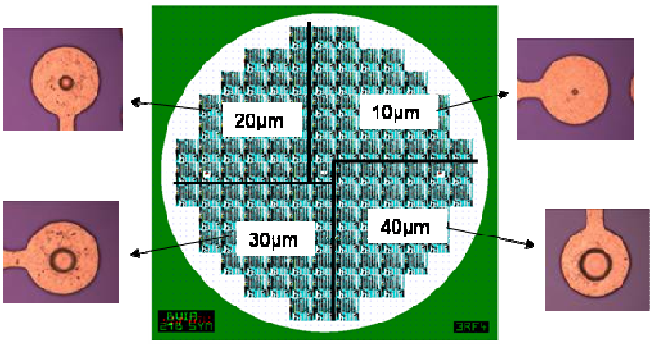


Figure 13: Dies layout for the 4 backside opening

The first electrical was a single TSV structure, a Kelvin structure. The mapping of the mean resistance value is displayed on Figure 14. First of all, one can notice the excellent yield of 98% for the TSV bridge. The impact of the backside diameter is obvious: the smaller the via bottom diameter, the larger the resistance. The via bottom diameter corresponds to the contact area.

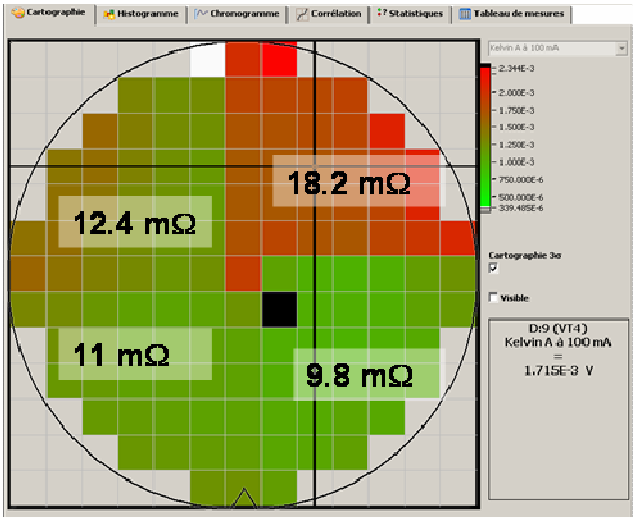


Figure 14: resistance mean value per backside diameter for single TSV (Kelvin measurement)

From these measurements, we can extract the resistance of the TSV bridge with the formula $R_{via} = R_{via\_top}+R_{via\_bot} + A_{contact}/(Pi*R\^2)$, where $A_{contact}$ is the contact resistance between via_top and via_bot. We extract from the Figure 13 the values R_{via_top} = 9.5mΩ and $A_{contact}$ = $4.7*10^{-9}$ Ω.cm^2. Very low contact resistance for Cu-cu contact is around 10^{-8} Ω.cm^2 [11]. Our contact resistance is slightly higher, due to the presence of ~200nm of Ti ($40*10^{-8}$ Ω.m), 20 time more resistive than copper. However, the total resistance of the TSV is always below 20mΩ, which is an excellent value for Si interposer and package applications.

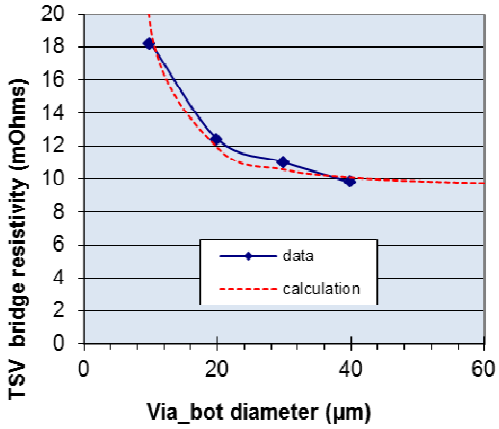
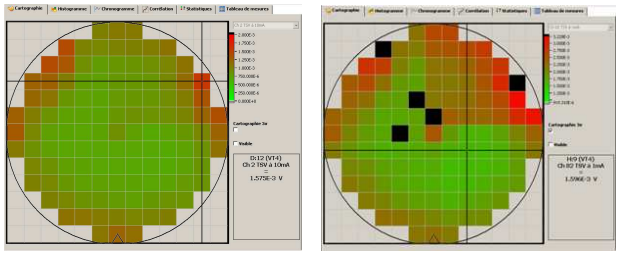


Figure 15: resistivity vs contact area curve for TSV bridge

Electrical tests on daisy chains are plotted on Figure 16 for 2 and 82 vias daisy chain. The yield is 100% for 2 vias and 95% for 82 vias. The impact of the via bottom diameter is still visible. Depending on the specification and the layout, the resistivity of the TSV bridge can be adapted with the diameter of via bottom. The leakage current between 2 vias and 6 vias have been measured under 50nA under 10 Volts. This meets the requirements of current interposer. A thicker insulation layer



2 vias 82vias

Figure 17: resistance mapping for TSV daisy chains for 2 (left) and 82 vias (right), 92 mΩ and 2.07 Ω respectively

Reliability tests must now be performed on this promising TSV bridge structure as well as C-V measurements.

Conclusion

We have developed and fabricated a new type of Through-Silicon-Via in order to meet thick interposer specifications for Si package applications. Mixing the advantages of both via-last and via-first technology, the TSV bridge offers a generic process flow to address AR up to 5 for thickness above 200µm. Most of the AR

comes for via top which can be processed on bulk wafer. The TSV bridge is kept low-cost since CMP step is excluded, and add only a backside additional lithography for via bottom in term of number of step. Same process flow can be used to reach 300µm deep via, increasing only the depth of via top.

The electrical test shows a very good yield and behavior. This TSV bridge, coupled with a standard multiple level Damascene routing layers offers new possibility in 3D integration.

Acknowledgements

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