Advanced lithography and electroplating approach to form high-aspect ratio copper pillars

Keith Best, Rudolph Technologies
Roger McCleary, Rudolph Technologies
Rudolph Technologies, Inc.
Wilmington, MA, U.S.A.

Keith.Best@rudolphtech.com

Richard Hollman, TEL NEXX
Phillip Holmes, TEL NEXX

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000793/2257193/isom-2015-thp23.pdf by guest on 22 November 2022

Abstract

Advanced packaging technologies continue to enable the semiconductor industry to meet the needs for ever thinner, smaller and faster components required in mobile devices and other high performance applications.

In the early days of advanced packaging, C4 solder bumps were the alternative to wire bonding. Although lead-free solder remains one of the preferred methods for assembly, tall copper structures (copper pillars) are becoming the standard interconnect solution for many applications. A process of lithography and subsequent electroplating are the mainstream process for today's copper pillar formation on wafer level for high-end flip chip devices.

The latest trends in advanced packaging require another technology development when it comes to copper pillars. Modern integration schemes such as 2.5D interposer as well as 3D stacking have pushed the limits of standard lithography and copper electroplating capabilities. Specifically, the need for fine-pitch high aspect ratio copper pillars represents a challenge. In addition, the trend towards rectangular panel-based packaging as seen with glass interposers or panel fan-out (P-FO) devices demands a challenging scale-up of lithography and electroplating equipment and processing capabilities.

This work specifically focuses on the formation of high-aspect ratio copper pillars in excess of 100µm by means of stepper-based lithography followed by electroplating. A unique test vehicle has been created to evaluate the process latitude for lithography for different resist materials as well as the specific electroplating challenges associated with these tall and narrow structures. The paper investigates the influence of key parameters such as CD uniformity, pattern density variations and resist profile on the critically important pillar height uniformity across the wafer or panel. In addition, the resist profile behavior at the substrate interface is being examined as it influences undercut behavior during wet etch of the plating seed layer. A number of wet and dry-film resist materials and appropriate lithography processes (spin coat or laminate, expose, develop) followed by copper plating based on varying chemistries and process parameters are being explored.

The paper also summarizes the current requirements for the above mentioned lithography and plating processes as seen in the industry today.

Key words

Advanced Packaging, 2.5D, 3D, TSV, High Aspect Ratio Cu Pillar, Stepper, Panel, Si Interposer, thick resist, dry-film resist, sidewall angle, Through Silicon Via, Electro-Plating, ECD, Cu plating

I. INTRODUCTION

Recent years have seen rapid development in the area of advanced packaging. In general, advanced packaging processes are concerned with the interconnection of multiple chips in a single package, providing increased functionality and performance in a smaller volume.

System Scaling Technology—the combination of front-end, middle-end and back-end to advance microelectronic systems—utilizes many different advanced packaging approaches, one of which being the concept of 2.5D packaging.

The term "2.5D packaging" has not always been used consistently throughout literature. The definition used for the purpose of this paper can be summarized as following [1]: A 2.5D package utilizes an interposer between multiple silicon dice and a system-in-package (SiP) substrate, where this interposer has through vias connecting the metallization layers on its front and back surfaces (Fig. 1).

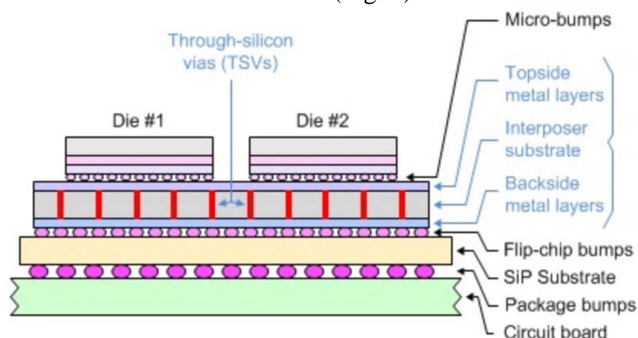

Fig. 1: A 2.5D IC/SiP using an interposer and through vias

Often, advanced packaging processes are adaptations of front-end processes. Their development is being driven primarily by the rapid growth in mobile handheld devices such as smartphones. A number of technologies are in development or in production, including wafer level chip scale packaging, copper pillar bumps on through silicon vias (TSVs), fan-out wafer level processing, and many more. Of particular interest is the replacement of solder bumps by fine pitch copper pillar bumps, this has been the subject of many new SiP designs. This paper investigates the lithography and plating of various copper pillar critical dimensions (CDs), with focus on heights in excess of 100µm and 25µm CD, in anticipation of possible future SiP requirements.

II. COPPER PILLAR BUMP TECHNOLOGY

The increase in I/O count has exceeded the pitch capability that traditional solder bumps can deliver and an alternative technology is required. For interposers, the key enabling technology has been the development of fine pitch copper pillar bumps to provide the high-density interconnection between the interposer and the die. Copper pillar bumps provide a number of advantages over the solder bump technology they are supplanting. They can deliver fine pitch down to 40µm, and less has been demonstrated; they also provide superior electromigration performance for high current carrying capacity applications.

Lithography and electroplating for fine pitch copper pillar bumps can be particularly challenging. The pillars are electroplated into openings in a thick layer of photoresist which exceeds the capability of most front-end tools. Typically, today's copper pillars range from 30-50µm in height, with aspect ratios from 1:1 to around 2:1

This paper describes the lithography system, resist process, electroplating system and process, required to create 5:1 aspect ratio copper pillars with heights in excess of 100µm.

III. EXPERIMENTAL DETAILS

A. Test reticle layout

In order to generate the required 5:1 aspect ratio structures, a customized test reticle was built to include a wide range of via CDs (copper pillar mold resist structures) and pitches. Fig. 2 shows a summary of the selected reticle module layout and content.

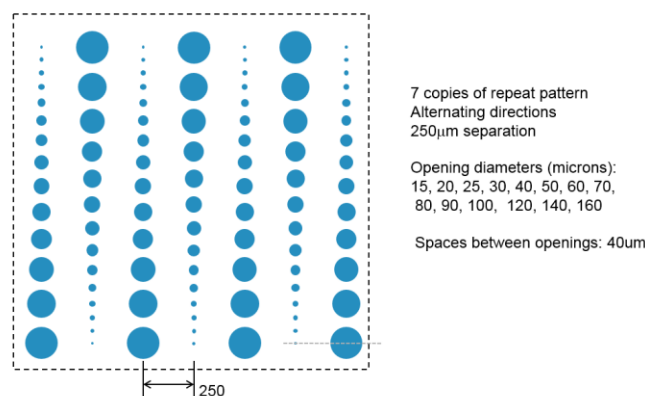

Fig. 2: Reticle pattern layout

B. Photoresist process

A negative tone photoresist, JSR THB-151N, was chosen for this work, its acrylate groups cross-link on exposure and are developable in industry standard 2.38% TMAH developer. The photoresist was spun to a thickness of 120µm on 300mm silicon wafers with under bump metallization (UBM) prepared seed layer. To reach the 120µm photoresist film thickness, two coatings of photoresist were required, soft baked at 130C, 300secs and

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000793/2257193/isom-2015-thp23.pdf by guest on 22 November 2022

130C, 360secs respectively. After coating, the photoresist film was allowed to rehydrate for one hour prior to exposure on the Rudolph Technologies JetStep® wafer stepper.

C. Lithography system

When processing a thick photoresist, well controlled sidewall angles are a critical requirement, especially when electroplating tall copper pillars. Most front-end tools have high numerical aperture (NA) lenses with low depth of focus (DOF) that prevent adequate penetration of thick films with sufficient image contrast to achieve the side wall angle and resolution requirements. Mask aligners also struggle with high aspect ratio imaging, not because of their NA, but because they are unable to provide the necessary focus offset required to penetrate the film at high resolution, limiting their ultimate aspect ratio and side wall angle control. Although photoresist sidewall angles are primarily a function of the photoresist material and its processing (pre-bake, post-bake, developing, etc.), the exposure system plays an important role. Accurate focus control across the wafer or substrate is required to achieve consistent and accurate CD control with straight and perpendicular side walls.

The lithography stepper employed in this study was a Rudolph Technologies JetStep® W2300 System (Fig.3). The system utilizes "on the fly" focus control to ensure that every exposure is at the optimum focal plane height. This capability is essential when advanced packaging substrates become warped by film stress and thermal cycling. The system's 0.1 NA provides a very large depth of focus DOF to maintain image integrity and CD control through thick films, a priority for high aspect ratio imaging when films exceed 100µm. The stepper lens is achromatized and the installed "filter wheel" provides the user a choice of illumination wavelengths to expose the photoresist layers. Specifically, the user has the ability to image at either "broadband" ghi (350-450nm), gh (390 to 450nm) or i-line (365nm) wavelengths. For this particular application, with the photoresist thickness of 120µm, high energy illumination of >1000 mJ/cm2 was required, so broadband illumination (g,h,i wavelengths) was employed to maintain high throughput.

Fig. 3: JetStep® W2300 lithography system

D. Exposure and develop process

The JSR THB-151N coated wafers were exposed using a focus exposure matrix (FEM) wafer layout which provided a large number of programmed focus and exposure conditions at a fixed stepping distance to enable quick and efficient characterization of the lithography process window for any pillar CD. The matrix is described in Fig. 4.

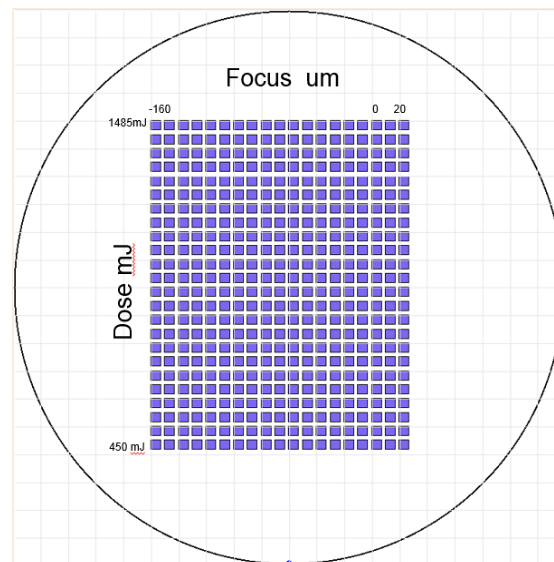

Fig. 4: Focus exposure matrix wafer layout

After exposure, the wafers were developed for a total time of 180 secs, using 6 puddles in 2.38% TMAH. A number of wafers were processed in this way to provide images of the resist structures prior to the electroplating process. The SEM micrograph in Fig. 5 shows a cross section of the photoresist via mold structures, the CD limit appears to be 25µm with this process, since the via is not open to the seed metal beyond this resolution.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000793/2257193/isom-2015-thp23.pdf by guest on 22 November 2022

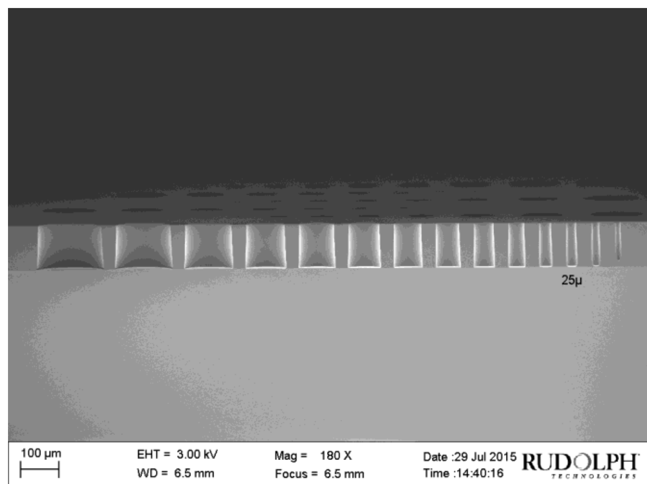

Fig. 5: SEM micrograph of photoresist via mold structures

It is interesting to note how the side wall angle of the photoresist changes with decreasing CD suggesting that the plating will generate a "pedestal" type of copper pillar base at larger CDs, becoming progressively more vertical at smaller CDs.

However, upon closer inspection of the smallest CDs, at higher SEM magnification, a slight "footing" can be observed at the base of the via (Fig. 6), and this could result in slight undercut of the final copper pillar. The footing effect was most likely the result of our unoptimized develop process.

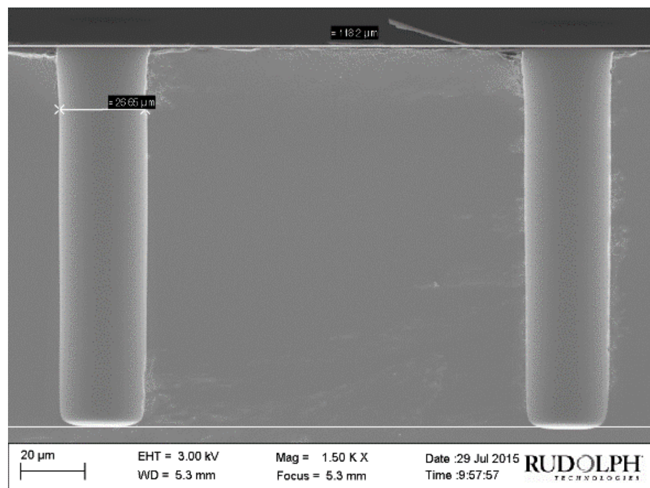

Fig. 6: SEM cross section micrograph of 25µm vias in 120µm of JSR THB-151N negative resist at 1215mJ dose

E. Electroplating system and process

After the lithography processing, the wafers were sent to TEL NEXX for electroplating. The plating process employed the TEL NEXX Stratus System (Fig. 7) which is a fully automated electrochemical deposition system for advanced wafer level packaging applications. The Stratus System deposits thick metal layers for wafer bumping, redistribution layers, TSVs, integrated passives, and MEMS. In addition to the system's industry-leading productivity, the vertical processing architecture eliminates defect sources associated with trapped bubbles, and non-uniform diffusion boundary layers inherent to horizontal plating cells. The Stratus P300 tool provides up to 30 ECD plating positions along with dedicated rinse stations which enables exceptional flexibility in a small footprint.

In this particular study, the TEL NEXX Stratus System used a methanesulfonic acid (MSA) copper chemistry with organic additives. The bath composition, operating temperature and current waveform were optimized for high speed copper plating into very thick resist features (up to 240µm) with flat bump profiles.

Fig. 7: TEL NEXX Stratus system

F. Resist strip process

The photoresist was stripped using an immersion bath with EKC162 solution at 60 degrees. The seed layer was not etched to preserve the profile of the photoresist mold.

IV. COPPER PILLAR RESULTS AND DISCUSSION

A. Electroplating results

The final copper pillar structures replicate the inverse photoresist mold profile (Fig. 8).

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000793/2257193/isom-2015-thp23.pdf by guest on 22 November 2022

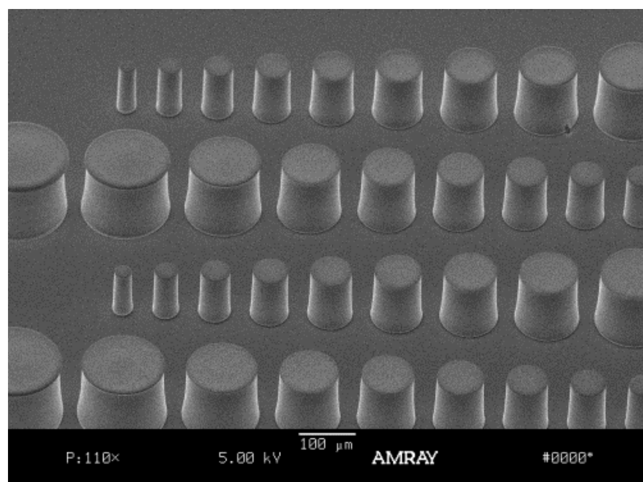

Fig. 8: SEM micrograph of electroplated copper pillars after photoresist strip

The electroplating process successfully deposited copper in the photoresist via "molds" that were open to the copper seed material to produce good quality copper pillars with a final minimum copper pillar CD of 20µm, indicating a process bias of 5µm. This bias enabled the final copper pillar to reach a 6:1 aspect ratio as shown in Fig. 9.

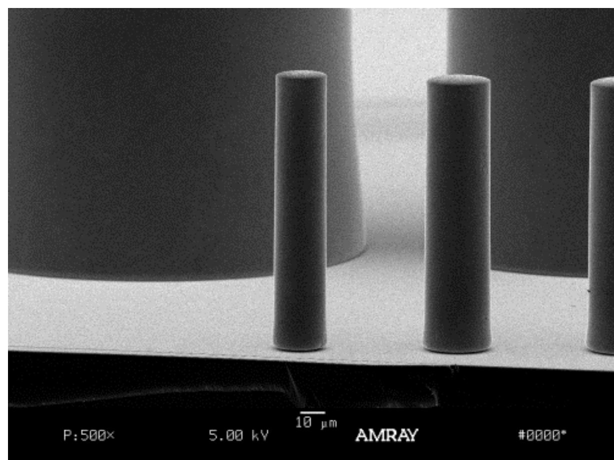

Fig. 9: SEM micrograph showing 20µm CD copper pillar with 6:1 aspect ratio

B. Lithography impact on copper pillar profile

The final copper pillars exhibit excellent side wall angle, 90 degrees for the smaller CDs. The profiles correlate with what was observed in the photoresist SEM cross sections. Specifically, the change in profile at the base of the photoresist for the smaller CDs resulted in a slight undercut of the final copper pillar. The removal of this photoresist foot could be achieved by either increasing the descum time or modifying the develop recipe. Conversely, the larger copper pillars tended to flare out slightly at the base (Fig. 10) compensating for any undercut. This will benefit the structure during the removal of the copper seed layer.

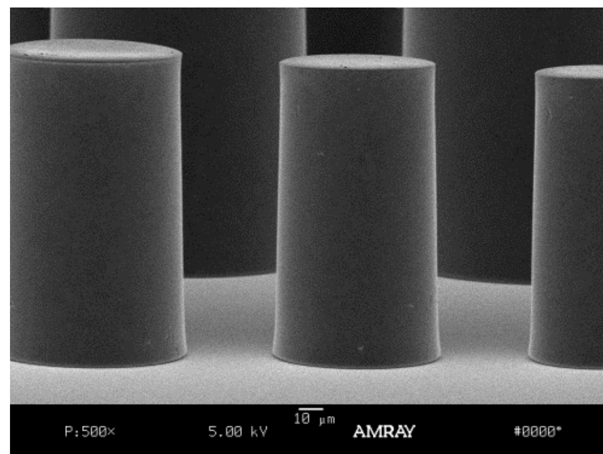

Fig. 10: SEM micrograph of larger copper pillars showing same base profile as photoresist images

C. Electroplating copper pillar rheology

The rheology of the copper pillar surface is very important for bonding reliability and the uniform plating of Sn solder, which was not performed during this particular study since it was not the primary objective. Fig. 11 shows the flat top surface of a copper pillar which is free of voids and defects.

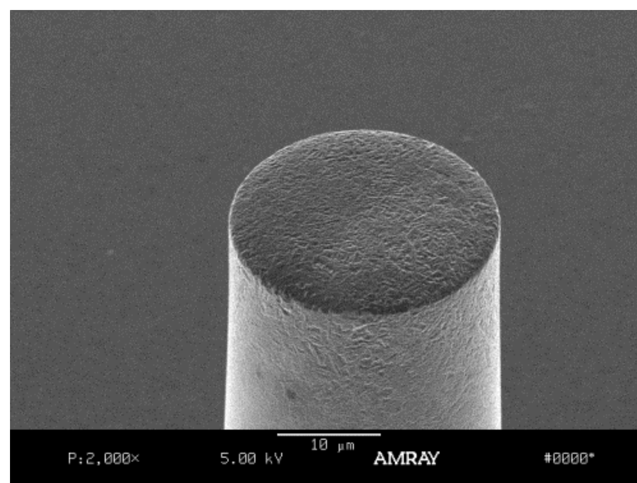

Fig. 11: SEM micrograph of copper pillar top

D. Importance of CD control on copper pillar height

For advanced packaging applications, precise copper pillar height control is essential, and lithography CD control plays an important part in the plating process since CD variation directly affects plated height. The electroplating rate is proportional to current per unit area, i.e. the open area at the bottom of the photoresist openings at the beginning of the process, and the area of the evolving metal surface during deposition. Variation in CD or sidewall angle across the

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000793/2257193/isom-2015-thp23.pdf by guest on 22 November 2022

wafer will result in a corresponding change in copper pillar height. For example, in the case of copper pillar features a 5% change in CD can cause a 10% change in plated height.

V. CONCLUSION

The results of this study prove that it is possible to fabricate copper pillars more than 100μm in height, with aspect ratio up to 6:1, using advanced packaging stepper lithography in conjunction with electroplating systems. As advanced packaging requirements continue to evolve, the ability to image smaller copper pillar CDs, at reduced pitch in thick films, will provide increased I/O density opportunities for SiP designers. Furthermore, it is clear that maintaining good CD control, throughout the entire photoresist profile, is essential to achieving consistent copper pillar height which directly impacts the yield and reliability of the final package.

Acknowledgment

The authors wish to thank Corey Shay and Mike Thompson (Rudolph Technologies) for generating the lithography structures required for the electroplating process and the photoresist SEM micrographs for this paper. In addition, special thanks to JSR Corporation, Microelectronic materials, for supplying the JSR THB-151N photoresist for this study.

References

[1] Clive Maxfield, EE Times Article, 4/8/2012: “2D vs. 2.5D vs. 3D ICs 101”

[2] Toward 2.5/3D Packaging Enablement through Copper Pillar Technology Deborah S. Patterson *Amkor Technology*. Volume 16, Number 3 May - June 2012

[3] Ron Huemoeller, AMKOR Technology, Architectural Success of 2.1D & 2.5D, SEMI 3D Summit, Grenoble, France, January 2014

[4] J. C. Mack, “Fundamental Principles of Optical Lithography,” Wiley, 2007.

[5] Tom Strothman, STATSChipPac, Encapsulated Wafer Level Package Technology (eWLCS), ECTC 2014, Orlando, FL.

[6] M. Juergen Wolf, Fraunhofer IZM ASSID, 3D Technology as a Holistic Approach, SEMI 3D Summit, Grenoble, France, January 2014

[7] Klaus Ruhmer, RUDOLPH Technologies, lithography challenges for 2.5D interposer manufacturing, ECTC 2014, Orlando, FL, USA

[8] Jim Zhang, Richard Hollman, Zhenqiu Liu and Arthur Keigler, Cu Pillar Electroplating Process Control for Wafer Level Packaging, IWLPC Proceedings 2010.

[9] Akihisa Sekiguchi, Cristina Chu, Tokyo Electron. “From mobile electronics to the Internet of Things: Tokyo Electron Limited on the evolution of advanced packaging in memory and logic,” www.i-micronews.com, July 9, 2015.

[10] S. Golovato, T. Barbera and K. Fujita, Tokyo Electron. “Conformal Barrier/Seeds for Next-generation TSV Filling by Electroplating,” Chip Scale Review, vol. 18, no. 1, pp. 24-27, Jan.·Feb. 2014.

[11] A. Keigler, J. Chiu, Z. Liu and D. Goodman, Tokyo Electron. “Seed layer deposition in microscale features,” US Pat. Pub. US2012/0152752 A1 2012.

[12] J. Chen, K. Fujita, D. Goodman, J. Chiu and D. Papapanayiotou, Tokyo Electron. “Physicochemical Effects of Seed Structure and Composition on Optimized TSV Fill Performance, Proc. IEEE 65th Electronic Components and Technology Conference (ECTC), 566 – 572, 2015.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2015/1/000793/2257193/isom-2015-thp23.pdf by guest on 22 November 2022