Using Physics of Failure to Predict System Level Reliability for Avionic Electronics

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Abstract

Today's analyses of electronics reliability at the system level typically use a "black box approach", with relatively poor understanding of the behaviors and performances of such "black boxes" and how they physically and electrically interact. Box level analyses tend to use simplistic empirical predictive models, and the effort is typically driven by cost and time constraints. The incorporation of more rigorous and more informative approaches and techniques needs to better understand and to take advantage of the advances in user interfaces and intelligent data capture, which will allow for a broader range of users and for similar resource allocation. Understanding the Physics of Failure (PoF) is imperative. It is a formalized and structured approach to Failure Analysis/Forensics Engineering that focuses on total learning and not only fixing a particular current problem. It can involve material science, physics and chemistry; also variation theory and probabilistic mechanics. The approach necessitates an up-front understanding of failure mechanisms and variation effects. In this paper we will present an explanation of various physical models that could be deployed through this method, namely, wire bond failures; thermo-mechanical fatigue; and vibration. We will provide insight into how this approach is being accepted by system assemblers, as it allows for failure oriented accelerated testing, for substitution or "what if" analyses in lieu of the traditional accelerated life testing. This paper will also provide insight into a process to develop viable test plans and a tool that facilitates the entire process so that minimal testing is performed, thus reducing costs and schedule impacts. Examples of this approach will be presented.

1. INTRODUCTION

An avionics electronic assembly is a complex interaction of materials that depends on the harmonious interface of their various mechanical, thermal, and electrical properties.

It is widely known and understood that the overall cost and quality of a product is most influenced by decisions made early in the design stage. Finding and correcting design flaws later in the product development cycle is extremely costly. The worst case situation is discovering design problems after failures occur in the field. Implementing a newly developed reliability prediction analysis tool will forever change this equation. Before a single product is built, this valuable new tool enables the engineer to import the design files and quantitatively predict the life of the product according to the assumptions made for the user environment. The failure rate is predicted for thermal cycle fatigue of solder joints and plated through hole vias as well as shorting from conductive anodic filament (CAF) formation. The software will also produce a finite element analysis of the circuit board showing regions susceptible to excessive board strain during vibration or shock events. The most value comes from the ability of the engineers to perform various "what if" scenarios to determine the impact of any number of design choices. Finally, once the design has been optimized to satisfy the competing requirements, the software can be used to predict the rate of failure over the lifetime of the product and this information used to more accurately plan for the warranty and maintenance costs. With margins shrinking in the electronics industry, OEMs depend more on profits from extended warrantees. Inaccurate life prediction can cut heavily into this income stream. Under prediction of the failure rate will lead to cost overruns while over estimating failure will mean lost business to competing extended warrantee plans and the setting aside of funds that could instead be used for further product development. This presentation will demonstrate the capabilities and value that this new tool provides to the various functional units within an avionics electronics manufacturing company.

2. ENVIRONMENTS

The Navy, for example, has created three categories for the anticipated environments that their electronics may be subjected to.

Protected Environment

The protected environment is applicable for parts employed according to the following provisions:

a. used in readily accessible maintenance applications
b. used in a controlled environment
c. with a temperature range of 0°C to 70°C

d. not used in an application with shock, vibration, pressure or moisture
e. not stored for later usage
f. with an application life-span of up to 5 years

Normal Environment

The normal environment is applicable for parts employed according to the following provisions:

a. used in inhabited applications
b. used in applications usually accessible for maintenance or replacement
c. used in an uncontrolled, but not extreme, temperature environment with a temperature range of -40°C to +85°C
d. used in an application having a minimal to low-medium controlled shock, vibration, pressure or moisture environment
e. can be stored for later usage (not to exceed 10 years)
f. with an application life span of 5 to 10 years

Severe Environment

The severe environment is applicable for parts employed according to the following provisions:

a. used in uninhabited environments
b. used at varying temperatures or temperature extremes
c. with a temperature range of -55°C to 125°C
d. used in an application having a medium to high shock, pressure, vibration, or moisture environment
e. can be stored for later usage (over 10 years)
f. with an application life span of 10 to 20 years

For the purposes of this paper, we will focus on the severe environment as these are the most difficult to assess during the design phase of an electronic LRU.

3. FLIGHT AVIONICS FAILURE MODES

It is commonly reported that the two major influences on failures in avionics come from thermal effects and vibration/shock and one of the harshest environments of any electronics...the avionics stack! Current avionics are packaged in smaller and smaller configurations that retain heat. They are also subjected to the chimney effect, where the heat from the bottom circuit card assemblies can rise throughout the entire LRU increasing overall operating temperatures. Similarly, design engineers are making greater use of surface mounted devices (SMT) to reduce size and weight. Although these devices use less power, they can be more sensitive to heat and thus failure.

In addition, the GAO recently released a report[1] that tin whiskers, wire bond failures and printed wiring board failures are the leading generic failure modes being encountered. Figure 1 also shows from the report the most common component failures.

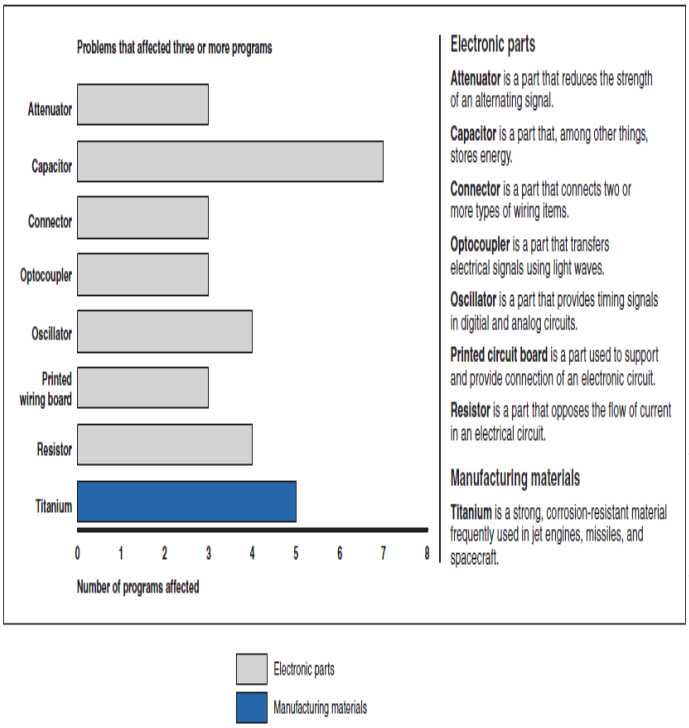


Figure 1– Most Common Device Type Failures Identified by GAO Report

Let's explore those failure modes and discuss the mechanisms that are driving these types of failures.

Tin Whiskers

Most of the electronics industry by now knows about tin whiskers. They know whiskers are slim metallic filaments that emanate from the surface of tin platings. They know these filaments are conductive and can cause shorts across adjacent conductors. And they know that these shorts can cause some really bad failures (see nepp.nasa.gov/whisker/ for a list longer than you need). But, with all of this knowledge, the industry is still struggling on how to predict and prevent these "Nefarious Needles of Pain".[2]

Whiskering occurs because of the presence of a compressive stress (or, more accurately, a stress gradient). This compressive stress drives the preferential diffusion of tin atoms. A few more things then have to occur for whiskers to form and grow, but in the absence of such stress, whiskering does not occur.

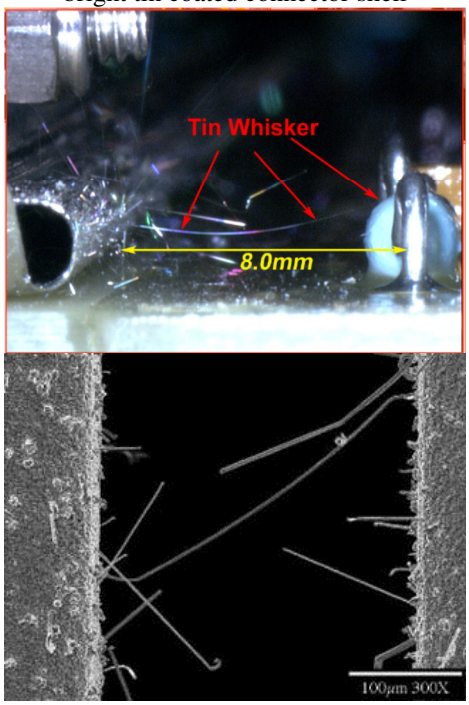
The stresses that drive whiskering derive from five sources:

- Base metal (intermetallic formation)
- Base metal (differences in coefficient of thermal expansion)

- Bulk plating conditions
- Oxidation/Corrosion
- External pressure

Whiskering occurs when one or more of these sources induce stresses of a sufficient magnitude. The magnitude of these stresses can be fixed at the time of production or can evolve over time. Figure 2 are examples.

Tin whisker growing from a bright tin coated connector shell



Courtesy of P. Bush, SUNY Buffalo

Figure 2– Examples of Tin Whiskering

Wire Bond Failures

Wire bonding has been the most common interconnect for IC packages for over 50 years. The most common materials are gold, aluminum, and more recently copper. The most common bond pad material is aluminum. A cross section of a typical wire bond is shown in Figure 3.

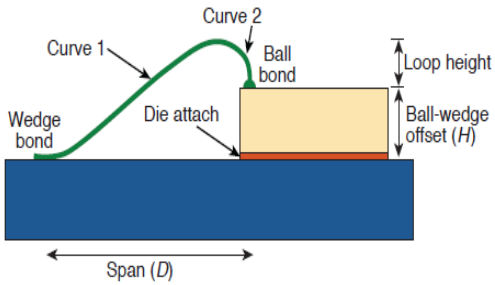


Figure 3 – Cross Section of a Typical Wire Bond.

Wire bonds tend to fail if exposed to elevated temperatures (intermetallic formation), exposure to elevated temperature and humidity (corrosion) and exposure to temperature cycling (low cycle fatigue).

Printed Wiring Board Failures

Printed Wiring Boards have several failure modes that are detrimental to reliable operation. Failures in PWBs can be driven by:

- Size (larger boards tend to experience higher temperatures)
- Thickness (thicker boards experience more thermal stress)
- Material (lower Tg tends to be more susceptible)
- Design (higher density, higher aspect ratios)
- Number of reflow exposures

The failure modes that can typically occur are Conductive Anodic Filament (CAF) shown in Figure 4 and plated though hole (PTH) Failures which can be driven by voids, etch pits or fatigue.

Conductive anodic filament (CAF), also referred to as metallic electromigration, is an electrochemical process which involves the transport (usually ionic) of a metal across a nonmetallic medium under the influence of an applied electric field. CAF can cause current leakage, intermittent electrical shorts and dielectric breakdown between conductors in printed wiring boards.

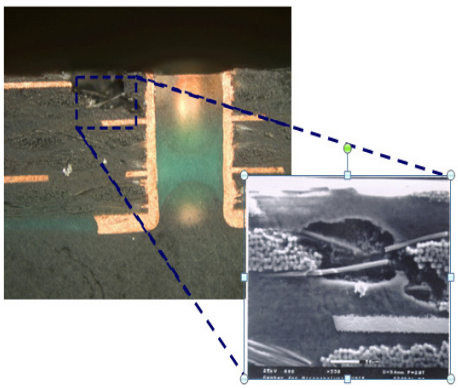


Figure 4 – Conductive Anodic Filament Failure

PTH voids can cause large stress concentrations, resulting in crack initiation. The location of the voids can provide crucial information in identifying the defective process; around the glass bundles; in the area of the resin; at the inner layer interconnects (aka, wedge voids) or at the center or edges of the PTH. Etch pits are due to either insufficient tin resist deposition or improper outer-layer etching process and rework. They can cause large stress concentrations locally, increasing likelihood of crack initiation and large etch pits can result in an electrical open.

Overstress cracking can occur in the PTH due to a Coefficient of Thermal Expansion (CTE) mismatch which places the PTH in compression. Pressure applied during In-Circuit-Testing (ICT) using a "bed-of-nails" can also compress the PTHs. Circumferential cracking of the copper plating that forms the PTH wall can also occur which is driven by the differential expansion between the copper plating (~17 ppm) and the out-of-plane CTE of the printed board (~70 ppm). Figure 5 illustrates these three failure mechanisms.

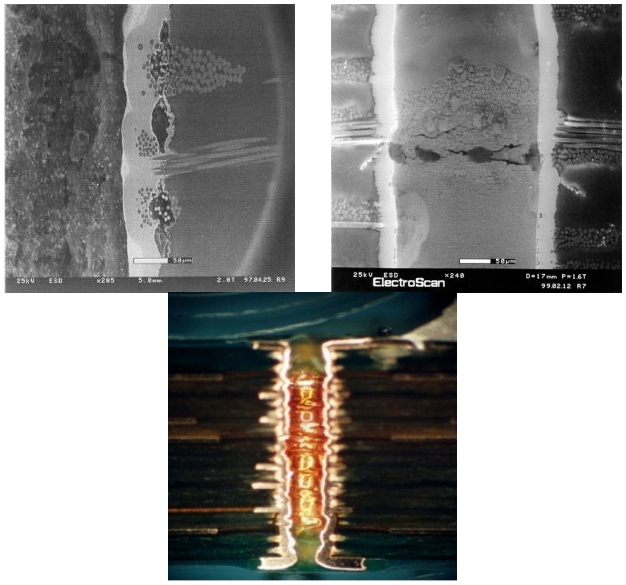


Figure 5 – Plated Through Hole Failure Mechanisms: voids (top), etch pits (center) and barrel cracking from fatigue (bottom)

Wouldn't it be an ideal scenario if you could determine during the design phase of your product whether it will survive the intended environments for its projected lifetime without incurring any of the noted failure mechanisms? You can accomplish this with an Automated Design Analysis Tool.

4. AUTOMATED DESIGN ANALYSIS

There are several high levels steps involved in running the software. They are:

- Define Reliability Goals
- Define Environments
- Add Circuit Cards
- Import Files
- Generate Inputs
- Perform Analysis
- Interpret Results

Reliability Goals

Desired lifetime and product performance metrics must be identified and documented. The desired lifetime might be defined as the warranty period or by the expectations of the customer. Some companies set reliability goals based on survivability which is often bounded by confidence levels such as 95% reliability with 90% confidence over 15 years. The advantages of using survivability are that it helps set bounds on test time and sample size and does not assume a failure rate behavior (decreasing, increasing, steady-state).

Defining Environments

Meaningful reliability predictions must take into account the environment in which the product is used. There are several commonly used approaches to identifying the environment. Approach 1 involves the use of industry/military specifications such as MIL-STD-810, MIL-HDBK-310, SAE J1211, IPC-SM-785, Telcordia GR3108, and IEC 60721-3. The advantages of this approach include the low cost of the standards, their comprehensive nature, and agreement throughout the industry. If information is missing from a given industry, simply consider standards from other industries. The disadvantages include the age of the standards, some are more than 20 years old, and the lack of validation against current usage. The standards both overestimate and underestimate reliability by an unknown margin.

Another approach to identifying the field environment is based on actual measurements of similar products in similar environments. This gives the ability to determine both average and realistic worst-case scenarios. All failure-inducing loads can be identified and all environments, manufacturing, transportation, storage, and field, can be included. In addition to thermal cycle environments, the software accepts vibration and shock input as well. Figure 6 shows representation of this input.

Vibration loads can be very complex and may consist of sinusoidal (g as function of frequency), random (g2/Hz as a function of frequency) and sine over/on random. Vibration loads can be multi-axis and damped or amplified depending upon chassis/housing.

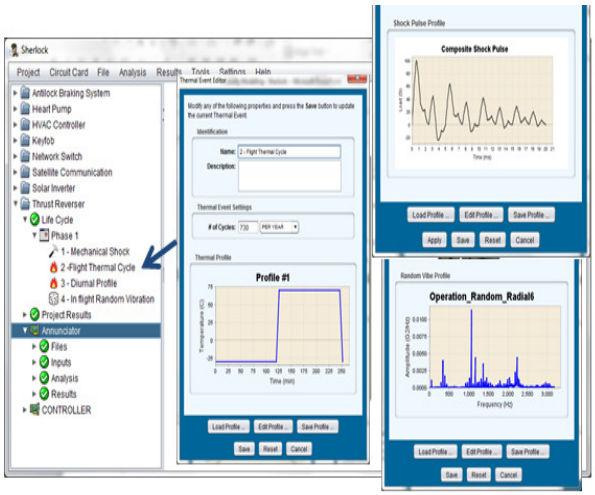


Figure 6 – Typical Stresses that can be Addressed in the Analysis

Import Files

The software is designed to accept ODB files which contain all the data for the PCB, the components, and their locations. The data can also be imported with Gerber files and an individual bill of materials. Figure 7 shows an example of a PCB stack-up and relevant data for reliability modeling. The software automatically generates the PCB stack-up, and its embedded database of Over 400 laminate materials having 48 different properties provides input to the models based on those selected.

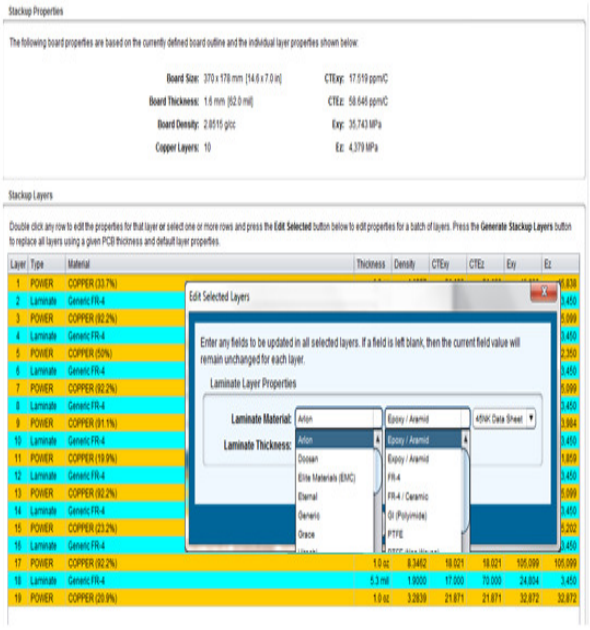


Figure 7 – PCB Stackup with Materials Database

Parts List

Individual component data is part of the ODB file, however, modifications to the data can be made manually to ensure the physical characteristics of all the components are accurate. Figure 8(a) shows the component editor while Figure 8(b) shows the components laid out on the board.

Figure 8 – Illustration of Parts List (a) on top and Board layout (b) on bottom

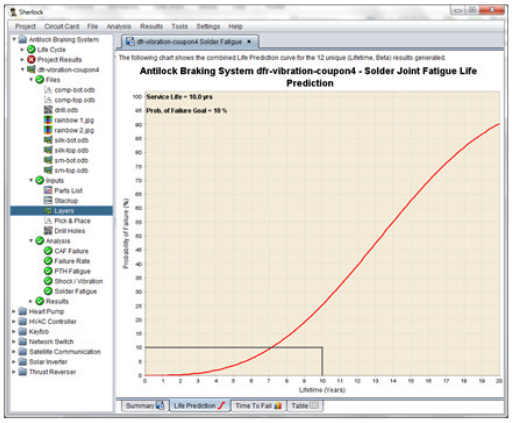
5. ANALYSES

Eight analyses are currently conducted:

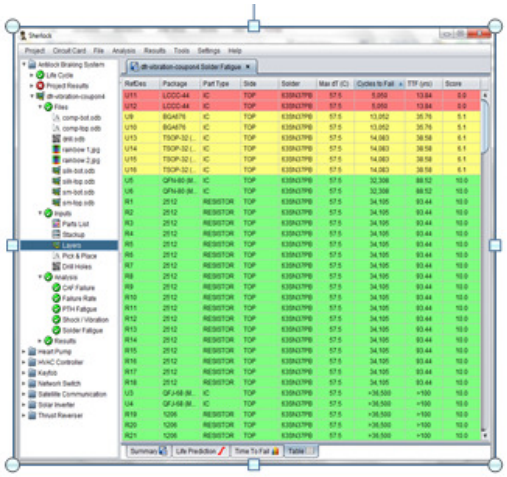
CAF – Conductive Anodic Filament Formation
Plated Through Hole Fatigue
Solder Joint Fatigue
Finite Element Simulations:
ICT Impact
DFMEA Natural Frequencies
Vibration Fatigue
Mechanical Shock

Figure 9 shows the output information can be illustrated either as an unreliability curve (a) , a parts list showing

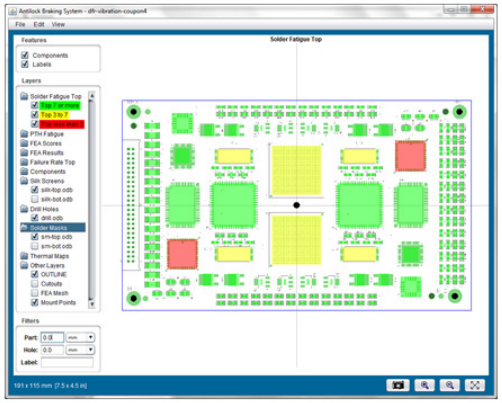
the discrepant parts (b), and the physical location (c). In the illustration shown, the failures are 2 ICs not meeting the overall reliability requirements specified as they are failing in 7 years rather than the necessary 10.



Unreliability Curve (a)



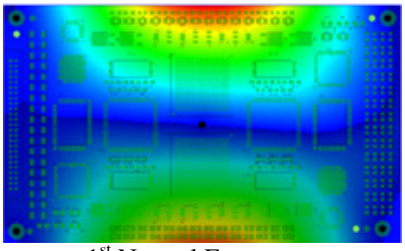
BOM (b)



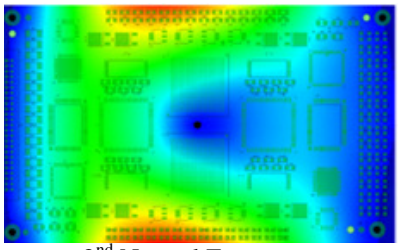
Physical Location (c)

Figure 9 –Illustrates the Ways that the Analysis Outputs Data

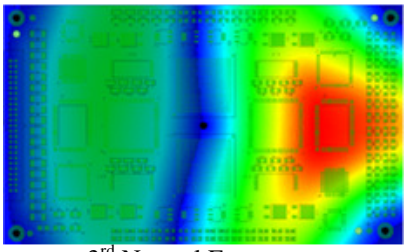
The software can also identify areas where natural frequencies impact the product design, as shown in Figure 10. It can provide a pictorial illustration of the stress locations for each of the natural frequencies identified.



1st Natural Frequency



2nd Natural Frequency



3rd Natural Frequency

Figure 10 – Natural Frequencies Identified

Knowing this information at the design stage permits the designer to make modifications to the layout such as hold down points, component placement, stiffeners etc. to assure compliance with the reliability requirements.

6 VALIDATION

It is difficult to provide insight into the complexity of the models used for the analyses but illustrating some of them will provide insight into the strength of the tool.

CAF is the migration of copper filaments within a printed circuit board under an applied bias. When the copper filaments bridge adjacent conductors, they can cause an abrupt, unpredictable loss of insulation resistance. When sufficient current is available, the mechanism can lead to burning and charring of the printed circuit board (PCB). CAF is influenced by electric field (voltage / spacing), temperature, humidity, laminate material, soldering

temperatures, and the presence of manufacturing defects (hollow fibers, poor wet-out, drilling damage).

The software benchmarks the printed board design and quality processes to industry best practices.

Design is assessed because of CAF's sensitivity to spacing and the increased influence of drilling damage at small separations between PTHs. In assessing the design, the software measures the wall-to-wall distance between the plated through holes (PTHs) along the orthogonal axes. The orthogonal axes (North, South, East, West) follow the weave of the glass fiber bundle.

Plated through holes (PTHs), also known as plated through vias (PTVs), are holes drilled through multilayer printed circuit boards (PCBs) that are electrochemically plated with a conductive metal (typically copper). These plated holes provide electrical connections between layers. Because these plated holes are metallurgically bonded to annular rings on the top and bottom of the printed circuit board, they act like rivets and constrain the PCB. This constraint subjects the PTH to stresses when the PCB experiences changes in temperature. PTH Fatigue is the circumferential cracking of plated through holes (PTHs) due to the differential expansion between the copper plating (~17 ppm) and the out-of-plane coefficient of thermal expansion (CTE) of the printed board (~45 to 70 ppm) during temperature variations.

PTH Fatigue is influenced by maximum temperature, minimum temperature, PTH diameter, PTH copper plating thickness, copper plating material properties (ductility, yield strength), printed board thickness, printed board out-of-plane material properties (CTE, elastic modulus), and defects within the copper plating (voids, folds, etch pits, etc.).

The software calculates a time to failure using the industry-accepted model published in IPC-TR-579, Round Robin Reliability Evaluation of Small Diameter Plated-Through Holes in Printed Wiring Boards.

Solder joints, also known as interconnects, provide electrical, thermal, and mechanical connections between electronic components (passive, discrete, and integrated) and the substrate or board to which it is attached. Solder joints can be a first level (die to substrate) or second level (component package to printed board) connection. This module assesses the thermo-mechanical fatigue behavior of second-level solder joints. During changes in temperature, the component and printed board will expand or contract by dissimilar amounts due to differences in the coefficient of thermal expansion (CTE). This difference in expansion or contraction will place the second-level solder joint under a shear load. This load, or stress, is typically far below the strength of the solder joint. However, repeated exposure to temperature changes, such as power on/off or diurnal cycles, can introduce damage into the bulk solder. With each additional temperature cycle this damage accumulates, leading to crack propagation and eventual failure of the solder joint. The failure of solder joints due to thermo-mechanical fatigue is one of the primary wearout mechanisms in electronic products, primarily because inappropriate design, material selection, and use environments can result in relatively short times to failure.

Thermo-mechanical solder joint fatigue is influenced by maximum temperature, minimum temperature, dwell time at maximum temperature, component design (size, number of I/O, etc.), component material properties (CTE, elastic modulus, etc.), solder joint geometry (size and shape), solder joint material (SnPb, SAC305, etc.), printed board thickness, and printed in-plane material properties (CTE, elastic modulus).

The software calculates a time to failure using strain energy. The detailed methodology is provided by the equations below. The first equation, shown below, describes the force exerted on a solder joint during a thermal cycle.

$$(\alpha_2-\alpha_1)\cdot\Delta T\cdot L_D = F\cdot\left(K+\frac{L_D}{E_1A_1}+\frac{L_D}{E_2A_2}+\frac{h_s}{A_sG_s}+\frac{h_c}{A_cG_c}+\left(\frac{2-\nu}{9\cdot G_b a}\right)\right)$$

where α is the CTE, T is temperature, L is one half component length, F is force, E is elastic modulus, A is effective solder joint area, G is the shear modulus, h is thickness and v is the Poisson ratio. The strain range induced in the solder joint during the thermal cycle is:

Sn3Ag0.5Cu --

$$\Delta\gamma = \frac{L_D}{h_s}\Delta\alpha\Delta T\cdot\left(\frac{D_{dwell}}{360}\right)\cdot e^{\left(2189\cdot\left(\frac{1}{398}-\frac{1}{T_{max}}\right)\right)}$$

The equations above are package-specific and account for the geometry, interconnect structure and material properties of the component and printed circuit board.

The stress on the solder joint is determined using the computed forces and this stress is combined with the strain to determine the energy dissipated by the solder during a thermal cycle through the following equation,

$$\Delta W = 0.5\cdot\Delta\gamma\cdot\frac{F}{A_s}.$$

The resulting strain energy is used to compute the number of cycles to failure for the component under temperature cycling using equations developed by Syed (see below).

Sn3Ag0.5Cu -- $N_f = (0.0019 \cdot \Delta W)^{-1}$

63Sn37Pb -- $N_f = (0.0006061 \cdot \Delta W)^{-1}$

Calculations have been made for each unique packaging format including, for example, BGAs, TSSOPs, passives, QFNs etc.

Unfortunately it is impossible to provide all of the validation equations and data in this paper and hopefully, this portion will provide adequate insight for the reader.

7. PRODUCT TEST PLANS

Product test plans, also known as design verification, product qualification, and accelerated life testing (though, these are not the same thing), are critical to the successful launch of a new product or new technology into the marketplace. These test plans require sufficient stresses to bring out real design deficiencies or defects, but not excessive levels that induce non-representative product failure. Tests must be rapid enough to meet tight schedules, but not so accelerated as to produce excessive stresses. Every test must provide value and must demonstrate correlation to the eventual use environment (which includes screening, storage, transportation/shipping, installation, and operation).

The critical first step is a good understanding of the use environment for the product. How well is the product protected during shipping (truck, ship, plane, parachute, storage, etc.)? How does temperature/humidity, thermal cycling, ambient temperature/operating temperature, salt, sulfur, dust, fluids, etc. as well as mechanical cycles (lid cycling, connector cycling, torsion, etc.) impact the product, particularly in an avionic application. Followed by the question - Do you have data or are you guessing? Product test plans are critical to the success of a new product or technology and must be stressful enough to identify defects and show correlation to a realistic environment. PoF Knowledge can be used to develop test plans and profiles that can be correlated to the field. This paper will provide insight into a process to develop viable test plans and a tool that facilitates the entire process so that minimal testing is performed, thus reducing costs and schedule impacts.

Figure 11 is an example of how the tool was able to provide an appropriate test time and test condition based on field environment and likely failure mechanism as an input to the customer for a product qualification plan.

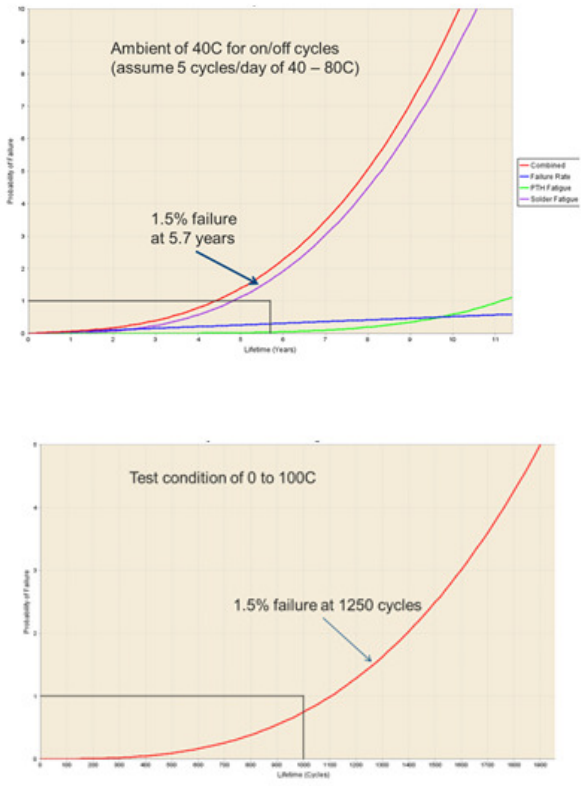


Figure 11 – Failures Curves on Top and Predicted Test Plan for Validating Data on Bottom

7. CONCLUSIONS

This paper has presented some of the issues associated with avionic reliability and a tool that can be used during the design phase of a project to mitigate those reliability issues

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1) U.S. Government Accountability Office, "Space and Defense Acquisitions – Periodic Assessment Needed to Correct Parts Quality Problems in Major Programs," GAO-11/404, June 2011
2) C. Hillman, G. Kittlesen, R. Schueller, "A New (Better) Approach to Tin Whisker Mitigation," DfR Solutions White Paper