Moisture Reliability Improvement of a High Performance Depletion Mode 0.15 um Gate PHEMT Process

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Abstract

Moisture reliability of a 0.15-um gate PHEMT technology for mm-wave applications was investigated. The PHEMT technology is fabricated with a deep UV optical lithography, and typically exhibits transconductance of ~550 mS/mm and fT of ~90 GHz.
Moisture reliability, THBL or BHAST performed at 85% relative humidity, and 95 ℃, or 130 ℃ and 85% RH, respectively, initially showed failures up to 70%, under various process splits. Extensive failure analysis pointed to a number of mechanisms contributing to failure, the key culprit being moisture ingress, enabled by poor quality of SiN, stresses, seams, and voids in the passivation dielectric around the gate topology. Moisture penetrated the SiN to GaAs surface through seams in the dielectric around the gate or regions of high local stress such as gate feeds and ends. A corrosion process ensued with the applied voltage bias on the device drain and gate during the THBL or BHAST environmental stress, leading to GaAs oxidation, metal migration and shorts.
By designing the gate topology appropriately, failures were reduced to the range of 0-3.4 %. Further, using a BCB overcoat, failures were completely eliminated.

Keywords: mm-wave PHEMT, Moisture Reliability, THBL, BHAST

INTRODUCTION

High performance PHEMTs for mm-wave applications requires submicron gate lengths under 0.25 um. Such devices have traditionally been fabricated with E-beam lithography instead of optical, since these dimensions are comparable to I-line optical wavelengths. E-beam lithography requires long exposure times for full 6-inch wafers. To reduce the gate process cycle time, and hence process cost, an optical DUV lithography process using Phase Shift Mask (PSM) was developed, yielding excellent devices with good uniformity and control on 6-inch GaAs wafers [1]. Typical FET characteristics had peak fT 86 GHz, Imax 575 mA/mm, Gmmax 520 mS/mm, gate pinch-off of -1.0 V, and breakdown, BVdg of 14 V. A travelling wave amplifier (TWA) with 10 dB gain up to 88GHz was manufactured with the process.

The initial process faced significant moisture reliability problems. 8mm FETs subjected to 1000 hr THBL (95 ℃/85%RH) or 96 hr BHAST (130 ℃/85% RH) with FETs biased at Vg=-2.5 V, and Vd=6V had failure rates based on leakage currents >0.1 mA/mm of up to 70%. This paper will discuss the failure mechanism and paths and enhancements of the process to yield no failures.

PHEMT PROCESS

The process uses PHEMT epitaxial material with 120 angstroms $In_{0.25}Ga_{0.75}As$ channel layer, sandwiched between an AlGaAs/GaAs supply layer and a superlattice buffer layer. Silicon pulse doping is used above and below the channel to achieve a relatively high channel sheet charge of about 3.25e12 e-/cm^2.

The process begins with forming 50 ohm/sq TaN resistor, followed by oxygen ion implant for device isolation. Ohmic contacts of Au/Ge/Ni/Au are evaporated and lifted. Source to drain spacing is 2.4 um. A wide gate recess is formed by mask and the N+ cap is dry etched. Gate formation comes next. After gate processing, silicon nitride is deposited to passivate the GaAs surface adjacent to the gate, contacts to Ohmic metal are opened, and a 0.8 um thick Au interconnect layer is formed using evaporation and lift-off. A capacitor dielectric of 1550 A SiN is deposited. Contacts to the gate metal

and first metal are opened, and a 4 um thick Au Airbridge metal layer is plated. A final nitride protective layer is then deposited.

GATE PROCESS

Critical to this submicron device reliability is the gate formation process and passivation. Details of the gate process have been discussed in 2011 GaAs IC symposium [1]. The process uses two steps to form the gate resist pattern. T-gates were initially examined, and subsequently changed to Y-gates. The gates are formed using DUV stepper combined with a strong phase shifting mask to expose a negative photoresist with underlying bottom anti-reflective coating (BARC layer), and developed. With short photoresist bake prior to second resist, the patterns are near vertical. Following BARC etch, a second conventional negative I-line resist was coated and exposed, and developed with a re-entrant profile for lift-off. The gate metal of Pt/Ti/Pt/Au/Pt/Ti was evaporated and lifted–off. The T-gate process suffered from wide CD variations. Moreover due to shadowing effect during evaporation of the gate metal, occasional voids were observed in the gate stem and under worse case incomplete gates were formed, that cannot be pinched-off during operation.

Y-shaped stems mitigating these effects were formed by flowing the bottom resist to create a smooth Y-shape pattern, then the BARC layer was etched using RIE, and the resist was baked again to prevent inter-mixing with subsequent second resist layer. To improve the CD uniformity and control, we developed a Lift-Off Resist (LOR) based second layer process where a thin, non-photosensitive polymer layer is coated on the wafer and pre-baked before applying a positive i-line resist on top. During develop after exposure, the LOR material undercuts the resist and forms a tri-layer lift-off structure for the metal lift-off.

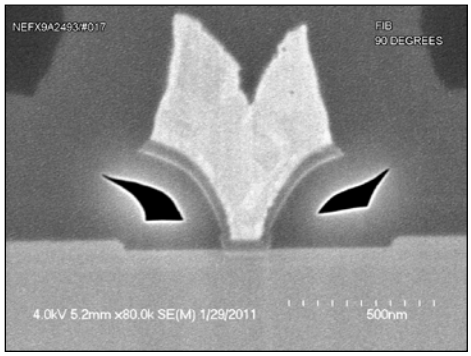

Figure 1. Y-gate Structure

The LOR material is based on PMGI (polydimethylglutamiride). The degree of undercut is a strong function of the LOR pre-bake condition. After both layers are formed the gate metal is evaporated and lifted –off. Figure 1 shows a typical Y-gate, and Table 1 and Figure 2 show typical FET characteristics.

Table 1. Key DC and RF parameters of 0.15 um PHEMT device

Parameter	Unit	Typical Value
Pinchoff voltage	V	-1.0
Peak Gm	mS/mm	520
Imax @ Vgs=+0.8	mA/mm	575
Ioff @ Vgs=-2, Vds=6	uA/mm	10
BVdg @ Ig=0.5mA/mm	V	14
BVds @ Id=0.5mA/mm	V	13
fT @ Vd=1.5, Ids=275mA/mm	Ghz	86
fT @ Vd=5, Id=100mA/mm	Ghz	40

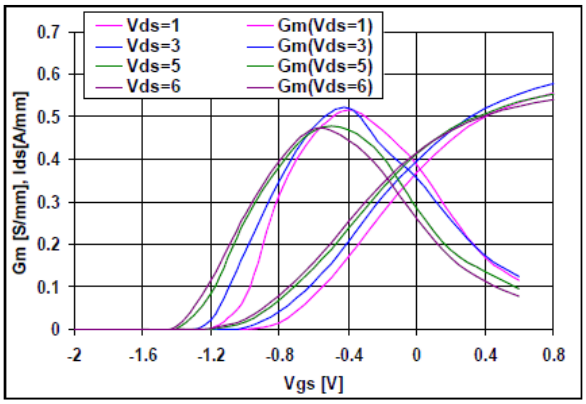

Figure 2. FET Id and Gm vs. Vg characteristics

MOISTURE RELIABILITY

Following device fabrication through the front-end process, the wafers received back-end processing, including back grinding, back vias, metallization, and dicing, and 2mm and 8 mm FETs were picked, packaged in 14 pin dips, bonded with 1 mil wire bonds. The 2mm and 8mm packaged devices were subjected to THBL (Temperature, Bias, and Humidity Leakage) test. A set of 8mm FETs were also subjected to BHAST (Bias, Humidity, Accelerated, Stress Test). The THBL tests were

performed at 95 °C/ 85 % Relative Humidity for up to 1000 hours, and BHAST at 130 °C/85% Relative Humidity for 96 hours or up to 144 hours. Prescreens of devices consisting of visual inspection, and electrical test were performed prior to the temperature, humidity tests, and typically drain leakages at Vg=-2.5 V, and Vd=6V were a few nano-amperes. Under these bias conditions and the environmental tests, failure rates were up to 70% under leakage criteria > 0.1 mA/mm. Table 1 shows typical THBL failure rates of die from four wafers from different lots with T-shaped gates and a final passivation of 4700 A SiN.

Table 1. THBL Fails of T-Gate PHEMTs

Wafers	2mm FETs #Fails/#Parts	8mm FETs #Fails/#Parts	Hours	Total Percent Failures
A	38/72	18/72	666	38.9
B	20/26	16/26	640	69.2
C	13/20	4/20	477	42.5
D	15/50	11/48	735	26.5

The failure rates are unacceptably high. BHAST also performed on the T-gate die tested at 96 hours and 144 hours showed a high failure. Table 2 shows BHAST results for 8-mm FETs with T-shaped gates and a final passivation of 4700 A SiN.

Table 2. BHAST results for T-gate 8mm FETs

Wafers	#Fails/#Parts At 96 hrs	#Fails/#Parts At 144 hrs	Total Percent Failures
E	8/27	13/27	52
F	1/20	3/20	15
G	1/18	7/18	38.9

Extensive failure analysis of failed devices indicated moisture ingress as major cause for the THBL fails. The sources of failure were: a) a poor nitride coverage of the device structure; b) high tensile stresses in the nitrides on the order of 350 MPA, which exacerbated seams, blisters, and potential cracks; and c) gate topology, which dictates the dielectric coverage.

Y-gates with narrow top CDs (<0.6 um) were found to result in significantly improved THBL and BHAST fails, however wide top CD (~0.8 um) Y-gates did not show significant improvement over T-gates, even though metal voids from shadowing effects were eliminated. Table 3 shows THBL results for 2mm and 8mm with wide top CD (~0.9um) and Table 4 shows results of FETs with narrow top CDs (0.6um)

Table 3. THBL results of Y-gate with wide top CD (~0.9 um)

Wafers	2mm FETs #Fails/#Parts	8mm FETs #Fails/#Parts	Hours	Total Percent Fails
H	25/40	33/40	1002	72.5
I	16/42	22/42	1002	45.2

Table 4. THBL results of die with Y-gate with narrow top CD (~0.6 um)

Wafers	2mm FETs #Fails/#Parts	8mm FETs #Fails/#Parts	Hours	Total Percent Fails
J	0/39	1/39	515	1.3
K	NA	1/106	515	0.9
L	1/58	1/56	515	1.8
M	0/47	0/48	515	0.0
N	0/36	0/35	515	0.0

Corresponding BHAST results of 8mm die with Y-gates and narrow top CD (~0.6 um) are shown in Table 5.

Table 5. BHAST results of die with Y-gate with narrow top CD (~0.6 um)

Wafers	#Fails/#Parts At 96 hrs	#Fails/#Parts At 144 hrs	Total Percent Failures
O	0/96	0/26	0.0
P	1/30	0/30	3.3
Q	0/30	1/30	3.4

Finally, with a thick (8 um) BCB overcoat deposited as final passivation over the 4700 A SiN, the failures on Y-gates with narrow top CD were completely eliminated. Figure 3 shows a completed cross-section and Tables 6 and 7 show THBL and BHAST results with the BCB overcoat. The BCB passivation were opened at pads only with thick photoresist and etched normally with SF6/O2.

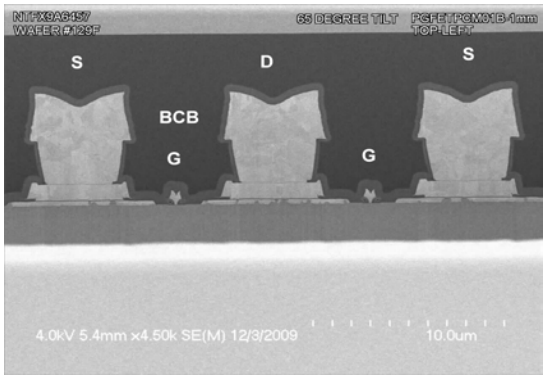

Figure 3. Cross-section of a completed Y-gate device with BCB overcoat.

Table 6. THBL results for 8 mm FETs with Y-gates and narrow top CD with final passivation of 4700SiN and 8um BCB overcoat.

Wafers	2mm FETs #Fails/#Parts	8mm FETs #Fails/#Parts	Hours	Total Percent Fails
U	0/38	0/38	1002	0.0
V	0/38	0/39	1002	0.0

Table 7. BHAST results for 8 mm FETs with Y-gates and narrow top CD with final passivation of 4700SiN and 8um BCB overcoat.

Wafers	#Fails/#Parts At 96 hrs	#Fails/#Parts At 144 hrs	Total Percent Failures
R	0/30	0/30	0.0
S	0/28	0/28	0.0
T	0/25	0/25	0.0

FAILURE ANALYSIS AND DISCUSSION

Scanning electron microscopy, and Focused Ion Beam cross-sections, as well as STEM and EDS were used to investigate failures. Moisture ingress was the major culprit. The paths for moisture ingress were dielectric seams, or cracks in the topology over or near the gate. High stresses in the dielectric could lead to cracks and blisters.

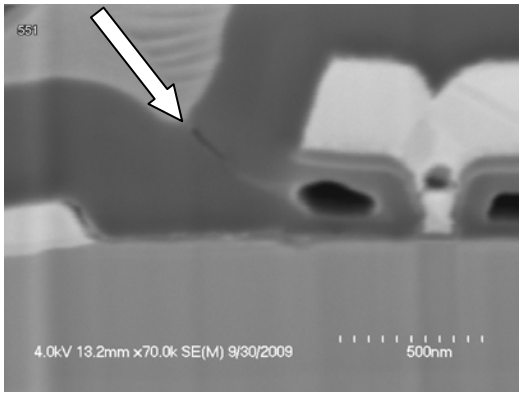

Figure 4. TEM image (TE-contrast) showing moisture ingress path and corrosion of GaAs surface of THBL failed T-gate PHEMT.

Figure 4 illustrates the void in the gate stem from metal evaporation, as well as poor dielectric coverage around the gate due to a wide top CD of the gate metallization. Moisture ingress has also resulted in oxidation of the GaAs surface. Further analysis tracing the moisture path through the passivation seam is shown in Figure 5, where the SiN in the path is seen to be rich with oxygen.

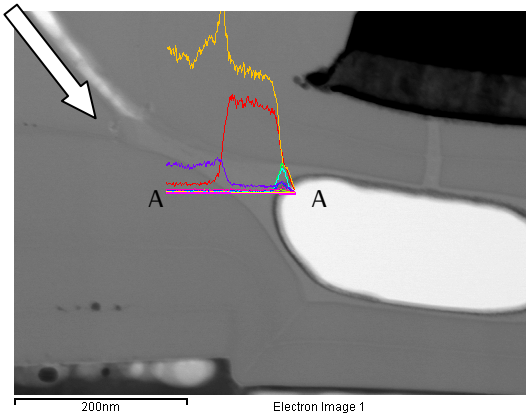

Figure 5. TEM Z-contrast image of moisture ingress through seam in dielectric along path indicated in SiN dielectric. STEM/EDS analysis was performed at location A-A indicated. Results shown in Figures 5 are expanded in Figure 6.

Moisture ingress leads to electrolytic corrosion [2] of the positive metal terminal, oxidation of the GaAs surface, and metal migration along the GaAs sub-surface leading to shorts. The dielectric path also shows a high concentarion of oxygen from oxidation of the nitride.

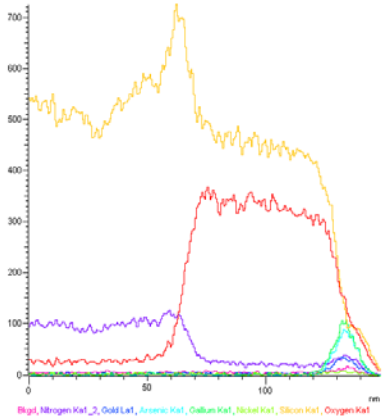

Figure 6. STEM/EDS analysis of moisture ingress path during THBL, indicating oxidation of the nitride.

CONCLUSIONS

Moisture reliability of DUV Lithography 0.15 um gates for mm-wave applications were improved by mitigating moisture ingress with proper gate topology with shorter top metallization width, and BCB overcoat. Y-gates eliminated voids in the

gate stem, and the shorter top metallization of Y-gates reduced the size of voids under the top part of the gate metal, which improved the dielectric coverage. THBL and BHAST fails initially as high as 70%, were eliminated by the improvement.

ACKNOWLEDGMENTS

The authors would like to thank Ed Ott, Les Szepesi, Tim Whetten and Lori Latta of Avago Fort Collins for THBL and Processing, and Peggy Cleary of Avago, San Jose for BHAST tests.

References

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