Assembly and Packaging Enabling System Integration

[1]Klaus Pressel, [1]Gottfried Beer, [2]Maciej Wojnowski
[1]Infineon Technologies AG, Wernerwerkstraße 2, 93049 Regensburg, Germany
Phone: +49-941-202-1321
Email: klaus.pressel@infineon.com
[2]Infineon Technologies AG, Am Campeon 1-12, 85579 Neubiberg, Germany

Abstract
More than Moore is a major trend to tackle the increasing difficulties of traditional Moore's law scaling. System in Package technologies, which allow heterogeneous integration, are appearing in ever more electronic applications. Furthermore we observe merging of silicon wafer technology with assembly and packaging technologies. Today a more coherent development taking into account chip, package, and the board is needed. In this paper we show how assembly and packaging can take up the slack because traditional More Moore downscaling is becoming more difficult. First, we introduce the Thin Small Leadless Package (TSLP) e.g. used in mobile systems. The TSLP is similar to the Quad Flat No-Lead (QFN) package, but thinner and with less parasitics. Second, we introduce wafer level type packages. The limits of standard wafer level packaging in respect to I/O counts pushed the development of the embedded Wafer Level Ball Grid Array (eWLB). We demonstrate the outstanding system integration capabilities of the eWLB including excellent mm-wave performance. For all the above mentioned packages chip and package technologies merge. They are door opener for nanoelectronic devices in respect to energy efficiency, mobility and security.

Key words
TSLP, eWLB, More than Moore, System-in-Package, passive integration

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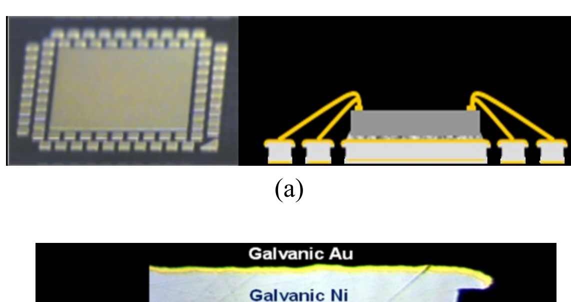
I. Introduction
Only few semiconductor companies are able to follow the ever more expensive path of Moore's law scaling. Today, we do not only reach cost constraints but also constraints in performance. New materials and innovative device developments are required. New developments in assembly and packaging help to keep the path. The trend towards More than Moore is of increasing importance [1]. More than Moore includes for example analog devices, RF devices, sensor and MEMS components, power chips, or bio-chips. These are technologies where Europe has a strong position. System in Package (SiP) is a rapidly evolving technology, which can combine More Moore and More than Moore devices. Driven by mobile communication SiPs appear more and more in mass production. Examples are not only combinations of processors and memory, but also SiPs that include sensors, MEMS, power electronic modules, camera modules etc. We observe an ever more merging of silicon wafer technologies with assembly and packaging technologies, and even with board technologies. A coherent development taking into account chip, package, and board is needed.

In this paper we provide examples of outstanding developments that emerged in assembly and interconnect technologies driven especially from Europe to tackle requirements for More than Moore. We start with introducing the so-called Thin Small Leadless Package (TSLP) of Infineon, a leadless package that can be made thinner than a Very Thin Quad Flat No-Lead (VQFN). The smaller contact height of the TSLP compared to VQFN cause less parasitics. A new leadframe design and the introduction of a fine filler mold material with adjusted coefficient of thermal expansion (CTE) played a key role for the TSLP package development [2]. Next we introduce developments in Wafer Level Packaging (WLP) type technologies. Limitations in pin count of standard WLP packages lead to the development of the embedded Wafer Level Ball Grid Array (eWLB). The eWLB technology is an approach which introduced new technologies like wafer level molding, but also technologies from the silicon wafer technology like lithography for thin film processing. We demonstrate the capability of the eWLB technology for compact system integration. SiP toolbox elements developed are vertical contacts, e.g. through encapsulant via

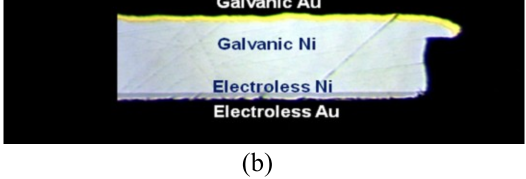
(TEV), double sided eWLB with two dielectric layers on both sides, integration of discrete passives, passives designed by special interconnect architectures, or integration of antennas into the package.
Another technology where Si wafer technology processes and assembly and interconnect technology processes merge is through silicon via (TSV) technology, because they need to be combined with a redistribution layer (RDL). TSVs allow short contacts, highest miniaturization, and shortest interconnects. A major trend is also chip embedding in board type laminates.
Continuous shrinking needs ever more process innovation for assembly and packaging. Development of compact package solutions with low parasitic effects requires introduction of new materials and understanding of interfaces. More and more complexity to manage them is an outstanding challenge today. Those companies that are able to manage the complexity in respect to compact system integration will be best in class.

II. Thin Small Leadless Package

For mobile devices extremely thin packages with low parasitics at high frequency are needed. Today, there is the trend for a package thickness of less than 1 mm. For tackling this need of extremely thin packages Infineon developed already early the TSLP package [2]. First approaches used wirebond solutions. Today, the TSLP package can be made as thin as ~0.3 mm and is then called TSSLP. Fig. 1(a) shows the footprint of a two-row TSLP and a sketch of the corresponding cross-section. Typically, the nickel based contact pin today is in the range of 30-50 µm high (Fig. 1(b)). For the TSLP packages an excellent



(a)



(b)

Fig. 1. (a) Image from the bottom of a TSLP (left), scheme of the cross-section (right), (b) example of a typical TSLP pin with a height of 50 µm. The package can be made as thin as ~0.3 mm.

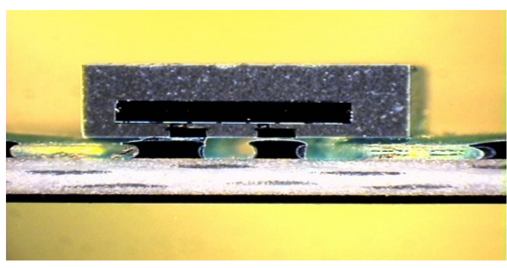


Fig. 2. Cross-section of the flip-chip version for the TSLP which leads to reduced losses and less parasitic effects.

high frequency performance has been demonstrated (see [3]–[5]). The package allows excellent heat transfer especially for the wirebond solution via the chip island. For the TSLP package development fine filler mold compound was investigated and applied to fill the narrow spaces.
The package was also investigated in respect to flip-chip applications (see [4], [5]). Fig. 2 shows the image of a TSLP with a flip-chip die. The application of flip-chip technology leads to reduced losses of the package and less parasitic effects, but has the disadvantage of less heat dissipation capability compared to wirebonding. Thus, depending on applications trade-offs need to be made. The set-up of the TSLP flip-chip version is very close to a standard WLP, but has the advantages of small contacts. Both wirebond and flip-chip versions are in production today for low pin count solutions.

III. eWLB for System Integration

A. From WLP to eWLB

Standard WLPs reach a limit in reliability for an area larger than 5 x 5 mm^2 when mounted on standard PCB. Reason is the different CTE of silicon, which is 3 ppm/K, and the PCB, which is around 15–18 ppm/K. For larger dice a costly underfill is required. Thus, the WLP package is for many applications I/O limited to < 60 I/Os, because a pitch of less than 0.5 mm on the board is hardly applied. Consequently, the embedded Wafer Level Ball Grid Array (eWLB) package has been developed that introduced a fan-out region. We distinguish between i) standard WLP, which is a fan-in solution that has no RDL, ii) Wafer Level BGA (WLB), which is a fan-in solution, but has a RDL and iii) the eWLB, which is a fan-out solution where the chips are embedded in the mold compound (see Fig. 3). The eWLB technology is for example introduced in [6].
The eWLB is a technology where silicon wafer technologies and assembly and packaging technologies merge. A thin-film for redistribution is directly applied on the chip. In chip design this can be treated as an additional BEOL, but with

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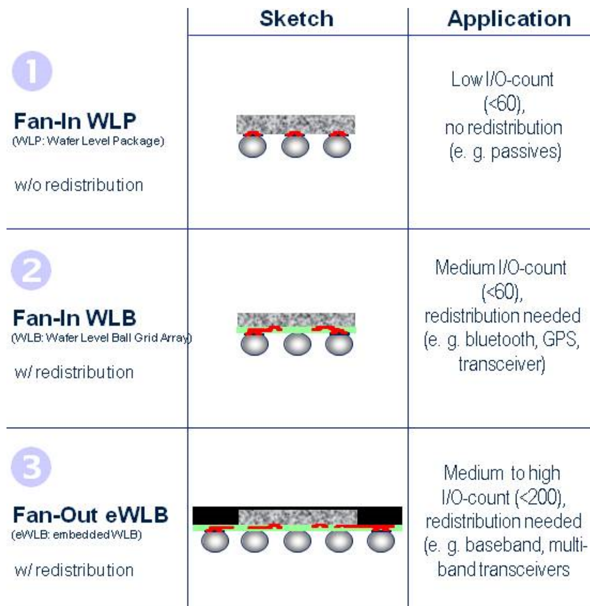

	Sketch	Application
1 Fan-In WLP (WLP: Wafer Level Package) w/o redistribution		Low I/O-count (<60), no redistribution (e. g. passives)
2 Fan-In WLB (WLB: Wafer Level Ball Grid Array) w/ redistribution		Medium I/O-count (<60), redistribution needed (e. g. bluetooth, GPS, transceiver)
3 Fan-Out eWLB (eWLB: embedded WLB) w/ redistribution		Medium to high I/O-count (<200), redistribution needed (e. g. baseband, multi-band transceivers

Fig. 3. Comparison of WLP, WLB, and eWLB solutions.

higher line/space (typically 20 µm/20 µm).

For development of the eWLB technology the experience on fine filler mold compounds achieved for the TSLP technology could be applied.

The eWLB package technology provides outstanding capabilities for system integration [7]. Below we introduce into latest technology developments that extend the SiP toolbox. We start with horizontal SiP solutions based on the eWLB technology and then move to 3D SiP integration.

B. Horizontal System in Package solution using eWLB

The eWLB technology allows to position two dice very close to each other. The image in Fig. 4 shows two dice with a spacing of ~300 µm to each other. The image shows that a mold compound with very small filler particles is applied, which have been improved during the last years. As the maximum filler particle size of advanced mold compounds today is less than 80 µm, chips can be brought together far below 200 µm. In addition these new mold compounds have CTEs of less than 10 ppm/K.

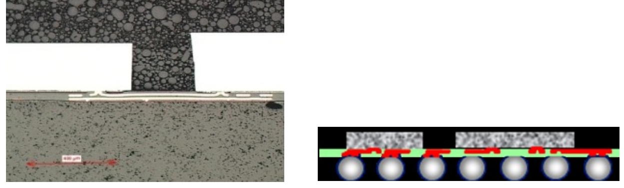

Fig. 4. Two chips side-by-side with a spacing of 300 µm.

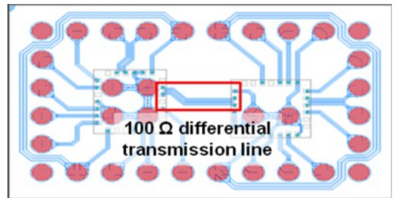

Fig. 5. Two chips side-by-side with matched transmission line for chip to chip interconnects.

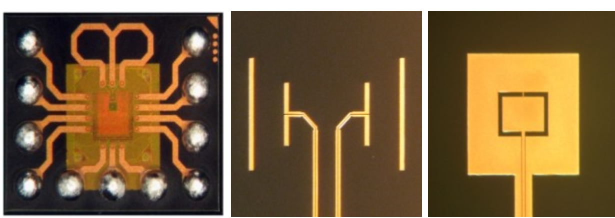

Fig. 6. (left) Example of a high-Q inductor in the eWLB fan-out region used for a 6 GHz VCO [9],[10], (middle and right) two different antenna structures in the eWLB fan-out region [11].

Design advantages exist for chips integrated in the same package and connected only by the RDL. One example is that we can design matched transmission lines in the package. An example of a 100-Ω low-loss differential coplanar strip line connecting two high-frequency chips is shown in Fig. 5.

It was demonstrated that the eWLB shows outstanding performance for mm-wave applications [8]. The eWLB fan-out region can be used advantageous for integration of passive components like inductors (see Fig. 6 left) or antenna structures (see Fig. 6 middle and right) into the RDL. The advantageous integration of an inductor for a 6 GHz Voltage Controlled Oscillator (VCO) was demonstrated in [9], [10]. Wojnowski et al. successfully presented antenna structures [11] in the eWLB fan-out region for a 77 GHz application.

C. Stacked System in Package solutions using eWLB

The eWLB technology opens excellent opportunities for 3D system integration. For 3D stacking, either using stacked dice or package stacking, vertical contacts through the mold compounds are required. Two different approaches have been investigated: TEV and laminate substrate bars. Typically for TEV the holes are drilled by a UV laser and filled with electroplating. The holes in the via bars are fabricated by a standard PCB process. The advantage of TEV is the higher density and higher design flexibility

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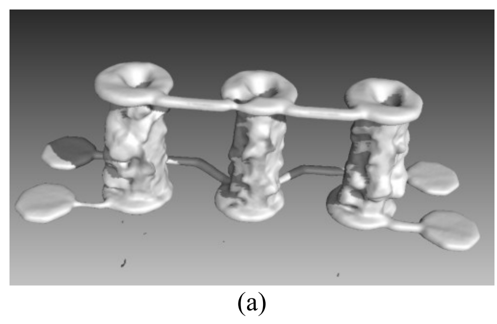
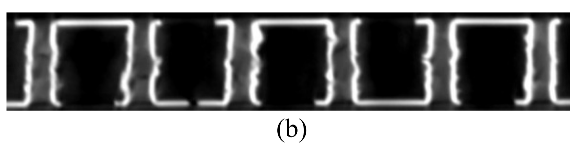


(a)



(b)

Fig. 7. (a) X-ray tomography of three TEV filled with Cu by electroplating, the TEV are connected via the RDL, (b) cross-section of a TEV chain with RDL on top and bottom.

compared to via bars. In contrast via bars are very cost efficient.

Fig. 7 (a) shows an X-ray tomography image of three 150 µm wide TEV filled with Cu by electroplating. X-ray tomography was applied advantageous for none destructive failure analysis to eWLB TEV structures. Thus, shorts and opens in TEV can be detected visually without destroying the package. Fig. 7 (b) shows the cross-section for a chain of six TEVs in an eWLB. For the eWLB, RDL can be

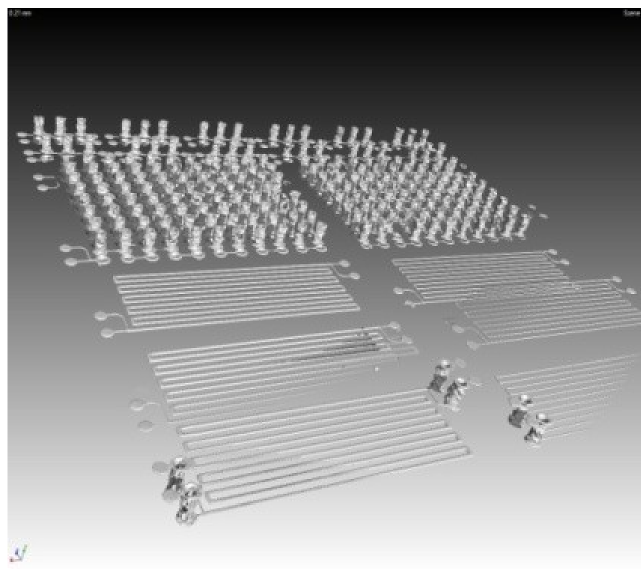
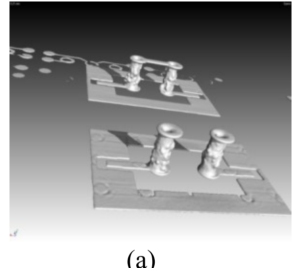
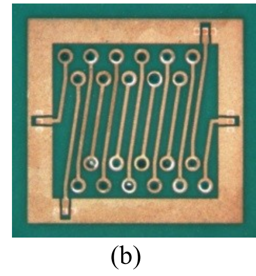


Fig. 8. X-ray tomography of TEV test structures for design of vertical passive components like inductors or transformers.





(a) (b)

Fig. 9. (a) X-ray tomography of TEV structures connected on top and bottom via the RDLs, (b) image of a solenoid transformer structure from the top.

designed on top and bottom of the package. Whenever possible a single layer RDL is applied because of cost reasons. They typically have a line/space of 20 µm/20 µm, but downscaling to 15 µm/15 µm is ready for introduction. Double layer redistribution on top and bottom side of the package can be realized.

Fig. 8 shows the section of an eWLB test wafer with various 3D test structures. Passive structures are designed using the TEV and connecting the TEV electrically by top and bottom RDLs. The designed test structures include for example inductors and transformers using vertical TEVs [12].

Fig. 9 shows test structures where TEVs have been used for design of integrated passive structures. The image in Fig. 9(a) made by X-ray tomography shows TEVs connected via the top and bottom RDL. Fig. 9(b) shows a transformer structure. Further details can be found in [12]. In addition to these design possibilities for passive structures and antennas in the WLB, there exists the capability for integration of discrete passive devices like inductors, capacitors or resistors.

Fig. 10 shows the example of a SiP solution applying

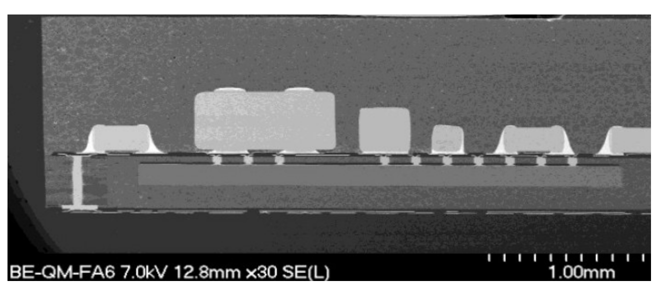


Fig. 10. Passive components mounted on the top RDL of an eWLB package. For this set-up the two dice were connected by their backsides. The active layers were connected to the bottom and top RDL, respectively.

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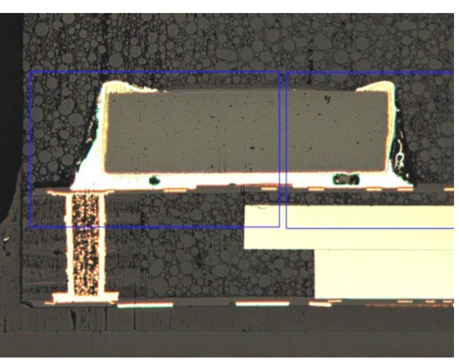


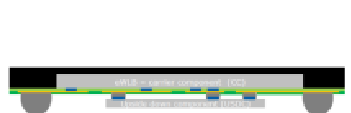
Fig. 11. Two dies with a thickness of less than 150 µm stacked in an eWLB. Advanced mold material allows filling also of regions smaller than 150 µm.

eWLB technology. Two dice were connected by their backside. The active sides of these dice were connected to the top and bottom RDLs, respectively. For both RDLs a double layer redistribution was applied. The two silicon dice only had a thickness of about 150 µm. An extremely thin package of thickness < 1.2 mm including the passives on top could be constructed. For this SiP example the vertical contacts were made by via bar based vertical contacts. On top of the upper RDL discrete passive devices were mounted. All the discrete passive components were attached by standard SMD processing to the pads of the Cu RDL.

A more detailed view of the SiP is shown in Fig. 11. The structure clearly reveals that filling with the mold compound under the thin 150 µm thin dice is achieved by a novel fine filler mold compound.

Another structure that is possible to design in eWLB technology is shown in Fig. 12. Two dice face to face can be mounted by using flip chip micro bumps of 40 µm size. In the eWLB RDL additional inductors were integrated.

The SiP examples presented here demonstrate the system integration design capabilities of the eWLB technology. Other technologies were silicon wafer level technology and backend merge are TSV and die embedding in laminate technologies. TSV technologies are typically combined with RDLs, e.g. for silicon interposer. They are presently investigated in worldwide consortia. A major hurdle for their broad integration is the cost issue. Chip embedding in laminate was investigated in the EU funded project HERMES. The capability to integrate extremely thin dice of less than 100 µm thickness into one package was studied.



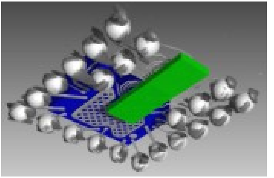


Fig. 12. (left) Scheme of two dice face to face in an eWLB; (right) X-ray tomography image of the two dice face to face in eWLB.

D. Importance of materials and failure analysis for eWLB

For development of the eWLB many material innovations were required. This included mold compounds with small filler size for side by side and stacked dice. The reduced CTE of the fine filler materials allows low warpage which is advantageous for package stacking. There are design opportunities to tackle hot spots and thermal balls. Crucial was the investigation of interfaces and their adhesion. The interfaces of silicon and mold compound as well as new dielectrica were studied. The understanding of the coherence of chip-package-board materials is crucial.

Miniaturization and system integration with new materials requires advanced failure analysis. In recent years a lot of new failure analysis techniques appeared with focus on assembly and packaging, especially for SiP integration. Examples are Lock-in Thermography (LIT), innovative Scanning Acoustic Microscopy (SAM) e.g. for GHz, Scanning Magnetic Microscopy (SMM) applying SQUID, or Focused Ion Beam (FIB) using plasma beams. All these new materials and analysis techniques require management of complexity.

IV. Conclusion

The SiP examples of this paper demonstrate that assembly and packaging using the eWLB technology offers outstanding system integration capabilities. This includes the integration of different chips, the design of integrated passives like resistors, inductors, transformers either in the RDL or using TEV advantageous. Antennas can be integrated in the package. But all these developments require a careful understanding of material physics. In the eWLB typical package materials were substituted by others. Fine filler mold compounds with adjusted CTE or new dielectrica for thin film technology are just examples. In addition the chips need to be designed such that they can be used for the eWLB technology, e.g. appropriate pad design. All these developments lead to a complexity that needs to be managed. TSLP, eWLB, TSV, and embedding in laminate are technologies where front-end and backend technologies merge together. These technologies provide the basis for applications towards energy efficiency, mobility, and security.

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