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Ultra-Fine Pitch Wedge bonding for Device Reliability Characterization

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Abstract

Intel's EM (electromigration) package level stress lab has historically used 1mil aluminum wire to bond to pads 53 µm by 60 µm, with a pitch of 86 µm by 88 µm. The lab was challenged to align its wedge bonding capabilities to match the pitch used at wafer level probing with a pad size of 30 µm by 37 µm and pitch of 43 µm by 50.6 µm. In order to achieve the 43 µm by 50.6 µm pitch, 0.7 mil aluminum wire and an ultra-fine pitch wedge was used. In this paper, the benefits or matching the wafer level probe card capabilities are discussed as well as the concerns and considerations of implementing such a small pitch process. The primary concerns are heel shorting and bond placement repeatability but many factors influence these parameters. A brief summary of electrical testing performed to validate the process is discussed as well as new challenges that have arose due to the new testing capabilities.

Key words
0.7 mil Aluminum wire, bond placement repeatability, destination bond rotation, electromigration, heel shorting, ultra-fine pitch, wedge bonding

I. Introduction

The rapid node scaling afforded by Moore's law has resulted in smaller and smaller device features. This potentially allows for higher densities of test structures per test chip or fewer required number of test rows to fully characterize the devices and process technologies. However, pad sizes and pitches, allowing access to test devices, do not scale at the same rate as the technology nodes due to limitations in the feature sizes and probe card pitch. Furthermore, the use of smaller pad sizes and pitches poses a challenge when wire bonding is utilized to characterize the devices, electrically. This is particularly true in the reliability testing of packaged devices wherein the devices are wire bonded to the frame of the CERDIP and subjected to extreme stress conditions such as high temperature, temperature cycling, and bake. It has been demonstrated that wedge bonding can be used down to 30 µm pitch using a 0.7 mil (17.8 µm) Al wire wherein the bonded wires are parallel to each other [1].

Intel's Electromigration (EM) package level stress lab has historically used 1mil aluminum wire to bond to pads 53 µm by 60 µm, with a pitch of 86 µm by 88 µm. The lab was challenged to align its wedge bonding capabilities to match the pitch used at wafer level probing with a pad size of 30 µm by 37 µm and pitch of 43 µm by 50.6 µm. This process allows for higher densities of test structures per test chip and fewer required number of test rows to fully characterize the devices and process technologies.

The capability to establish a 50.6 µm pitch process in the Y direction becomes quite challenging. The primary concern is heel shorting to the pad behind the bond foot. In Fig. 1, four locations of possible shorting are indicated.

The new process must withstand extreme stress conditions used in electromigration stress testing. The wire diameter reduction of 7 µm, necessary to support this fine pitch application, results in 51% decrease in wire strength and 76% reduction in stiffness [2]. The decreased strength and stiffness are critical mechanical properties that negatively impact performance and reliability [4]. Wedge bonding must be used for EM stress testing due to extreme heat exposure during such testing. Additionally, for the same pitch, a larger wire can be used in wedge bonding as compared to ball bonding which results in greater strength, reliability, and current carrying capacity [4].

In this paper, we present the 43 x 50.6 µm pitch wedge bonding process being used at Intel's EM/Device Stress Labs. With a pad size of 30 µm x 37 µm, the resulting increase in the number of test structures is approximately 2.6x that of the 86 µm pitch test row (with a pad size of 53 µm x 60 µm) currently utilized. At 43 µm by 50.6 µm pitch, we are able to maintain a toe-to-toe distance of 10 µm.

In section II, the advantages of the ultra-fine pitch process is discussed. In section III, the concerns and considerations are presented. Section IV presents the electrical testing that was performed to validate the ultra-fine pitch process could withstand the elevated EM stress testing conditions.

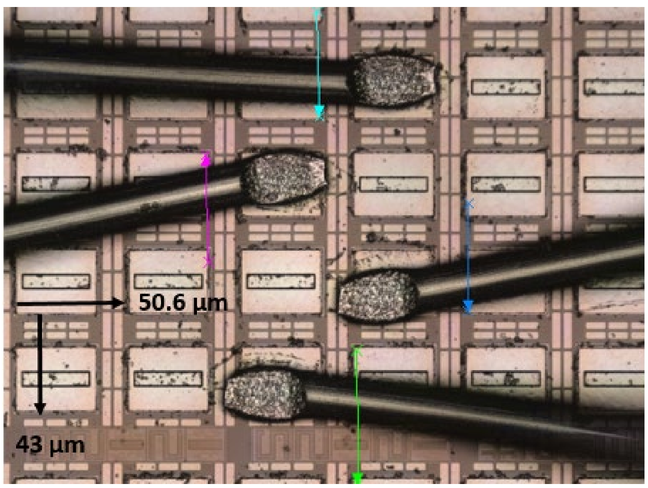

Figure 1. Four potential heel shorting locations (Keyence VK-X1000)

II. Benefits of Ultra-Fine Pitch Process

Intel's EM stress testing requires the assembly of the device of interest into a package (CERDIP). Testing of EM structures using test rows specifically designed for EM test assembly has been the normal process for several generations. Due to the high cost of silicon real estate, it is advantageous for the package level assembly process to align to wafer level probing capabilities to enable paired test data as well as reduce the amount of silicon area required and provide a common test row design.

Historically, package level EM testing has utilized wedge bonding of 1mil Al/Si wire on the Hesse Mechatronics BJ820 platform. The Silicon test material is comprised of 53 µm x 60 µm pads with a pitch of 86 µm in the Y direction and 74 µm in the X direction. The ultra-fine pitch process uses 0.7mil Al/Si wire and an ultra-fine pitch wedge to bond to pads 30 µm x 37 µm with a X/Y pitch of 43 µm /50.6 µm. Fig. 2 shows the ultra-fine pitch bonding to the larger, standard sized pads as well as the smaller pads.

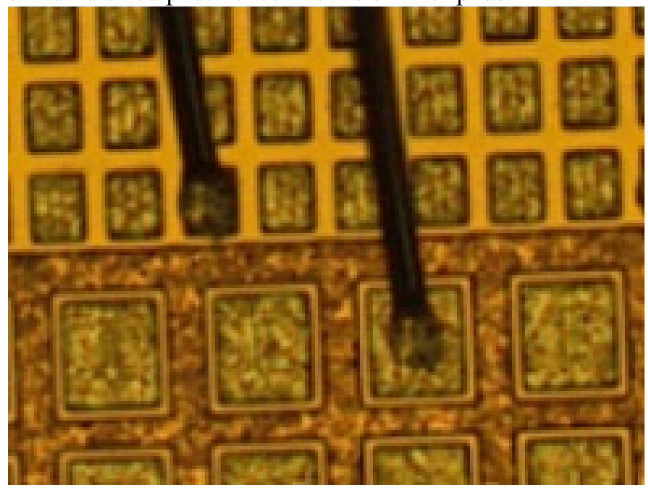

Figure 2: 0.7mil wire bonded to 30 µm x 37 µm pads (left) and 53 x 60 µm pads (right)

III. Ultra-Fine Pitch Process Considerations

The primary concern with the ultra-fine pitch wedge bonding process is heel wire droop shorting to the pad directly behind the destination bond foot. Many different considerations will affect the heel distance from the shorting pad. The main considerations are:

- Metrology to determine if shorting is present
- Shorting Test Material
- Bond placement repeatability
- Loop Height
- Destination bond rotation

A. Metrology Considerations and Test Material

Having a quick data turn method to determine if shorting is occurring is imperative. SEM imaging is time consuming and costly. Electrical shorting testing can be used, requiring appropriately designed test material that is an effective indicator of shorting risk, as well as an electrical test fixture that can test for such shorting. Using purely an electrical test fixture to screen for shorting, only provides a binary indicator of shorting and requires much more testing to inform shorting margin limits, as no dimensional information is provided by such tests. Combining the 2 items above together with a 3D microscope allows for quantitative limits to be set and used regardless of other factor such as wire length. Fig. 3 shows a 3D image of the same wires from Fig. 1 using a Keyence 3D microscope. The wire diameter of 0.7mil wire is 17.8 µm so any value measured at or below this value is automatically a short. The shorting margin will be the space between the wire and the shorting pad.

Utilizing 3D micrographs, the distance of the wire above the shorting pad can be calculated (Fig. 4) and used in conjunction with the electrical test fixture to determine quantitative process boundaries needed to prevent shorting. These quantitative limits can then be used when developing recipes regardless of the bond location. As the bond location moves farther away from the package, the loop height must be adjusted (increased) to accommodate the shorting margin limits.

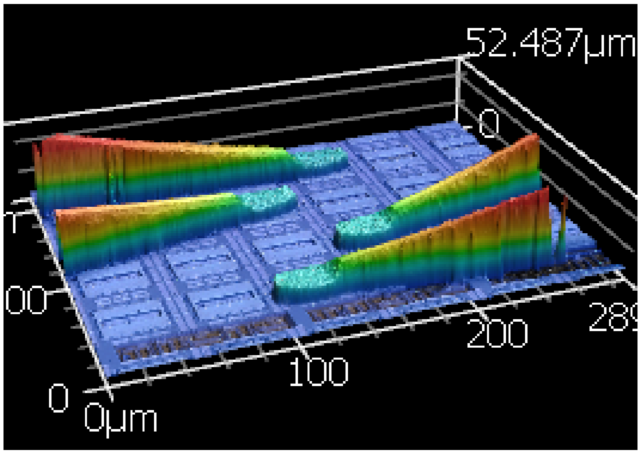

Figure 3: 3D image of wires from Fig. 1 (Keyence VK-X1000)

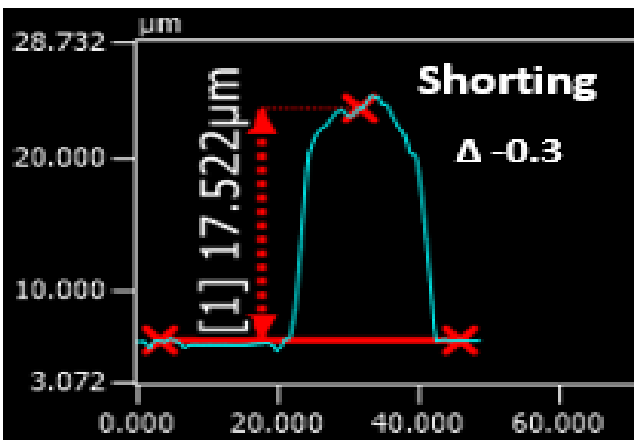

Figure 4: Wire distance above shorting pad confirms shorting (Keyence VK-X1000)

B. Bond Placement and Repeatability

Bond placement and repeatability are very important due to the extremely low shorting margins both to adjacent pads as well as the heel shorting pad. Bond placement and repeatability have several factors which influence the outcome on ultra-fine pitch wedge bonding. The primary driver for initial bond placement is a robust calibration procedures to ensure recipes do not need adjustments after calibrations are performed. Additional considerations are:

- Bonder screen resolution
- Material placement within the package
- Calibration
- Destination bond rotation

The ability to place the initial bond on the pad is limited by the bond tool screen resolution. The resolution on the BJ820 becomes quite pixelated when viewing 30 by 37 μm pads using the 2X objective. The magnification optics can be changed to help improve the resolution, however increasing the magnification~~,~~ decreases the field-of-view (FOV) which can have other repercussions based on assembly line controls. Changing from a 2X objective to a 4X objective, increased the image resolution by 50% but decreases the FOV of the image by 75%. As the FOV decreases, the ability to auto align decreases, compounded by the repeatability of the material placement within the package. If the placement repeatability has a very low tolerance such as using an automated pick and place tool, then the decreased FOV will have limited impact on the auto alignment capabilities. Alternatively, if a manual or highly variable process is used for die attach, the decrease FOV will have a negative impact on auto alignment capabilities due to reduced search distances.

Bond rotation at the destination bond is often required to prevent shorting to adjacent pads, toe to toe shorting, and/or to prevent adjacent bonds from being knocked off. Bond placement calibration is only valid for non-rotated bonds. Fig. 5 shows how bonds can shift when the destination bond is rotated. In order to account for the bond placement delta, the recipe bond locations must be manually adjusted by trial and error. The material placement repeatability within the package has a substantial impact on the bond placement with bond rotation. Therefore, using an automated pick and place tool with high placement repeatability is key to making a robust recipe. If a high variability material placement methodology is used, many units will need to be used to optimize the recipe. Even with the optimization of bond placement with high variability placement methodology, the yield will decrease as opposed to a high precision automated placement tool. Fig. 6 shows how bonds can shift from package to package when the material placement repeatability is not well controlled.

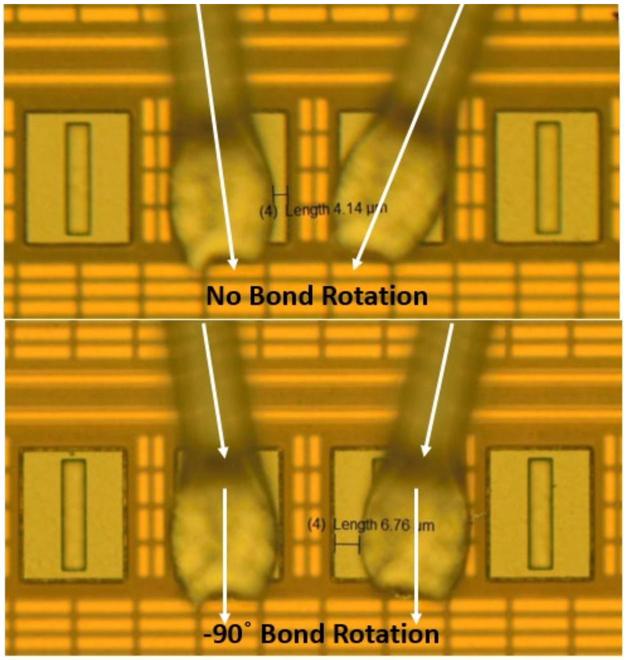

Figure 5: Bond rotation effects on bond placement

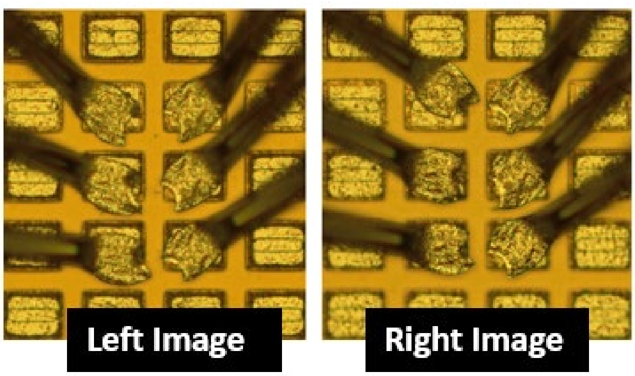

Figure 6: Bond placement repeatability with high material placement variability

C. Loop Shape and Height Adjustment

In order to increase the distance of the heel of the wire above the shorting margin pad, the loop shape and height must be optimized. The farther the bond pads are away from the lead frame, the harder it is to angle the heel high enough to prevent shorting. As the loop height increases, the wire has the potential to protrude above the package cavity. If the wires protrude above the package cavity, handling by operators becomes a major concern as the wires can easily be broken during handling as well as during package loading into EM stress boards. Another concern with protruding wires is the potential for damage induced by airflow. Optimizing the ultra-fine pitch wire shape, and height could result in a need to re-design the package to alleviate these concerns.

D. Electromigration Stress Testing

Optimization of the assembly process has to take into account the end-use for reliability testing. EM stress testing requires extreme temperatures as well as moisture testing [3] which could induce wire droop or other concerns affecting adhesion of the wire bond to the substrate. Initial pull strength data was collected validating that the bond strength was within tolerance. Bond strength does not take into consideration the high temperatures that the bonds experience during stress. 3 types of testing where evaluated and compared to the previous, conventional 1mil wide-pitch process. Adjacent bond Shorting, opens (due to bond adhesion failure) and paired stress data where evaluated.

Opens testing was performed by bonding to a slab of connected metal to test the bond adhesion. If the stress conditions induced bonds to experience failure of adhesion, the result would be the measurement of infinite resistance coincident with the event. Shorting testing was performed by bonding together pads that where electrically isolated from each other and adjacent to one another. This testing was used to look for wire shorting such as heel shorting, and toe to toe shorting. The final testing evaluated the established 1mil/86 µm pitch to the new 0.7mil/30 µm x 37 µm pitch processes. Paired structures where used to validate that the two processes where matched. Fig. 7 shows the matched stress data between the two processes. Paired EM stress testing was performed on various types of structures to ensure that it worked for a variety of normal testing that is performed in the business process. This paired test was a test-to-failure, due to electromigration, of a structure representative of our normal test structures and under common stress conditions.

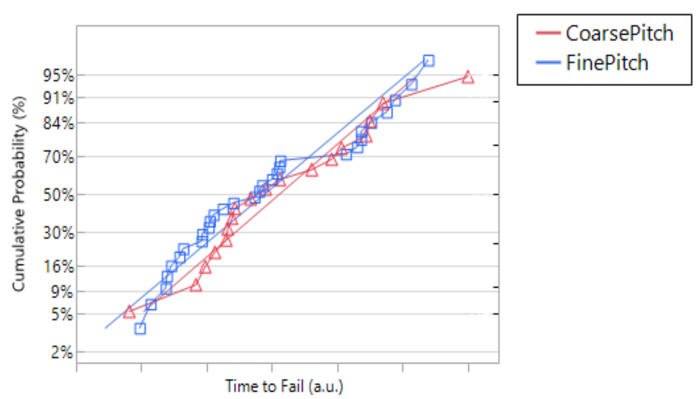

Figure 7: Reliability Stress Results between 0.7mil Al, 43 µm pitch test structures (blue) and 1mil Al, 86 µm pitch test structures (red).

IV. New Challenges

Ultra-fine pitch bonding has allowed bonding to additional test structures which previously could not be bonded to with the old fine pitch methodology. In some cases, the result of testing new structures, unforeseen consequences occurred which required extensive debug of the entire assembly process to determine root cause.

V. Conclusion

In conclusion, the 30 µm x 37 µm pitch wedge bonding infrastructure and process has been demonstrated to show very similar results to that of the 86 µm pitch wedge bonding infrastructure requirements and process in terms of bond quality, yield and reliability characterization. The challenges of heel shorting have been addressed using loop height optimization, bond rotation, and tighter assembly controls as well as a 3D surface microscope. The resulting impact of this 2x decrease in pitch is a 2.6x increased efficiency in the use of Si real estate.

The ultra-fine pitch bonding process will require much stricter assembly controls to ensure a stable and repeatable processes. Looping optimization and advancements will be critical to improving the process and driving the pitch down even further to keep pace with probe card capabilities.

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