Flip chip reliability and design rules for SIP module

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Abstract

The first part of this work is dedicated to the study of "system in package" (SiP) solutions based on different substrates, namely organic or silicon. Generally speaking a SIP is composed by several active and passive components stacked on an interposer. Benchmarks done by Safran have demonstrated that in terms of substrate, embedded die technology leads to several advantages compared to 3D TSV or TGV based packaging approaches. The benefits leaded by this substrate is the possibility to embed some Surface Mount Technologies, bare chips or integrated passives devices (IPD) banks directly above or below the stacked active components. This way, top and bottom surface of the substrate can be used to integrate several heterogeneous dies side by side while using low profile flip-chip assemblies on the C4 side. Finally, in this kind of 3D architecture, this embedded technology enable a gain of integration, without using costly TSV connections. Substrates of high quality allow a reduction of interconnection pitches leading to very aggressive integration.

Secondly, a 3D stack with 3 levels of components, as described above, means to, at least, 2 or 3 REACH compliant sequential assembly processes, depending on the needs. In order to consider all the solutions for an optimized integration and a high reliability, this work focused on the study of a simple SIP, which includes the top die assembled by flip-chip. For the flip chip hybridization, copper-pillars technologies are studied in the case of both organic and silicon interposers. The aim of this study is to understand in depth both processes and to obtain information on the reliability aspect after thermal cycling stress of the flip chip assembly.

Thirdly, we built many silicon test chips with different characteristics with a dedicated daisy chain test vehicle. The different parameters are: chips' thicknesses (50 to 200 µm), chips' sizes (2 to 8 mm), bump structures (diameter), and the pitches of the interconnection (from 50 to 250 µm) and the number of interconnection rows. Designs were chosen in order to fit real operational configurations. Moreover, these configurations are interesting to build a comprehensive model in order to understand the failure mechanisms. These chips are then stacked by flip-chip on the silicon and on the organic substrate. We are also designing the two configurations of substrates. Only the production of the organics part is outsourced.

Fourth, with all these configurations we will be able to fit the thermo-cycling test results with thermos-mechanical simulations done by finite elements. 3D models will take into account the different geometries in order to understand and quantify the various key parameters. The analysis will mainly focus on 3D interconnections. Design rules based on the results will be derivate. The aim is to obtain dimensional criteria based on stress versus deformation responses. Information obtained will be exploited for designing the future functional SIP.

Fifth, in order to assess the electrical behaviors of this 3D architecture, signal integrity aspect will be considered as well. As for the design, the migration from an existing 2D electrical design to a 3D architecture design will be studied keeping the signal transmission without any degradation.

The ultimate aim of this work is to define mechanical and electrical design rules that can then be used in functional SiP modules.

Key words

Copper-pillar, Flip chip, Mass reflow, System In Package

I. Introduction

Direction of study

In the aeronautical field, electronic integration roadmaps show that the weight and the volume of on-board electronics must be reduced for the most recurrent functions in the next few years. There are many reasons for this: on the one hand the need to reduce the size of electronic boards to save space and incidentally consume less and on the other hand the objective is to decrease the size of the electronics that accompanies the MEMS sensors. This would make it possible to place the systems closer to the equipment.

In this way higher level of integration and heterogeneous technologies are being developed today. To obtain this, components and assemblies are evolving. Increasingly, the choice is made to use unpackaged chips in order to gain in flexibility for implementing 3D architectures at the assembly level in particular with system in package (SIP) concept. At the same time the overall reliability needs to be further improved.

It is in this direction that our work is carried out, particularly for ASICs accompanying MEMS sensors or for reducing the footprint of the cards used for calculators.

Focus on current development on technologies for component assembly

The main directions for increasing electronics integration are briefly introduced. The transition from 2D to 3D has gone through the migration from a System on Chip (SoC) approach to a System in Package (SiP) architecture of the electronic components. As a first step 2.5 D has been introduced where the components are mounted on an interposer allowing them to be connected one to each other side by side and then connected to the board through fan-out redistribution layers. 3D is conceivable only when a component is mounted on another with through silicon via (TSV). Multiple assemblies are possible with the use of µbumps, TSVs. In addition, embedded dies in the packaging substrates is increasingly used to enhance the compactness of the systems. All these techniques have finally the same purpose, the miniaturization of electronics while increasing the performances.

Firstly, all these architectures are developed in order to reduce the foot print (rooting surface) occupied by the components, which in all fields of application is a major issue [1].

Secondly, 3D interconnections like TSVs and µbumps implemented at chip level shorten the lengths of interconnection and decrease the distance between the different components. These configurations improve the speeds in the connections and thus the overall performance [2].

Flip-chip assembly is one of the most important features for these types of packaging.

Focus on flip chip assemblies

For decreasing size and cost while increasing functionality the chip scale package (CSP) is a natural way for migrating from wire bond technology to flip chip technology. Traditional wirebonding shows limitation in the number of pins while for the same number of pins, flip chip technology authorizes having a chip with area 50% smaller [3].

The recent momentum to use flip-chip interconnections in microelectronics is also due to an evolution of the organic substrate manufacturing as well as of welding joint materials. The democratization in using copper-pillar, underfill and encapsulation materials participate in the adoption of flip-chip [4]. Practically these types of assembly need fine pitch organic substrates and µbumps which are the focus of this work.

Focus on copper-pillar

Copper-pillar technology is used for a long time for flip-chip assembly. System miniaturization using copper-pillar is already in many products. For example manufacturers like Flextronics or INTEL have fine pitch copper-pillars in their products [5], [6], [7]. Nevertheless, in the aeronautical field it is not fully adopted because of reliability concerns.

Today, µpillars with pitch of 10µm [8] exist, but not for flip chip assembly on organic substrate. Current publications show pitch below 30µm but this is only on silicon substrate, where CTE mismatch does not represent a limitation.

On glass substrate, as seen in publication from Infineon Technologies for example, [9], [10], pitches of 30µm with copper-pillars are also demonstrated. For this type of glass substrate CTE of 3.8 ppm/°C are used [11].

For organic substrates the state of the art gives more heterogeneous figures. Although a large majority is around 100 µm, it is possible to find assemblies with smaller pitches like for example Siliconware Precision Industries with 70µm [12] , IBM with 50µm [13], Institute of Microelectronics A*STAR with 30 µm pitch [14], or Amkor technology with 50 µm [15].

In works involving pitches of 50 µm or less, the use of the NCP technique is often present. For example thermal cycling reliability was successfully passed with copper-pillars of 30µm pitch and thermos-compression process on organic substrate with Cu bond pad [14]. However this NCP method seems to present some problems during thermomechanical reliability tests. Indeed, fillers entrapment is observed in the interconnects when solder cap are small, as can be seen in [14]. This problem causes failures during thermal cycling because cracks propagation initiates from the location where fillers entrapment occurs. For that reason, dispense of underfill will not be made with NCP method in this study.

II. FOCUS ON OUR WORK

This work reports new technological solutions to increase our ability to integrate more electronic components in a reduced volume. The aim is also to improve at the same time the overall system reliability.

As a general concept, SIP is composed by several active and passive components stacked on an interposer, with embedded die technology to reduce interconnection lengths. Both sides of the interposer can be used with flip-chip assemblies as describe on Figure 1 .

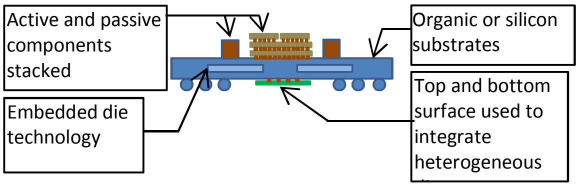

Figure 1: Global SIP module.

This work focuses on a simple SIP test vehicle which includes the top die, assembled by flip-chip with copper-pillars or gold-stud bump technologies on either an organic or a silicon interposer. The aim is to evaluate thermal cycling reliability and extract mechanical design rules from our test vehicle to help designing future functional SIP, this being in agreement with the needs of SAFRAN.

Flip chip Assembly

Configuration of a flip chip assembly is represented on Figure 2:

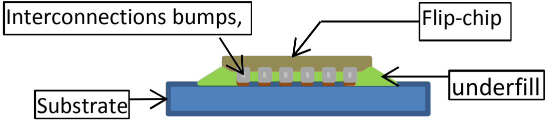

Figure 2: Flip-chip assembly.

Flip-chip assembly test vehicle can be characterized by four parts:

- The chip in silicon, which is used for daisy chain test.
- Organic or silicon substrate used to complete the daisy chains and allows electrical test.
- Bumps with solder to connect the chip on the substrate.
- Underfill is used to fill the space between the chip and the substrate.

Chip design

The choice was made to produce the silicon chips at LETI, Grenoble. These are daisy-chained test vehicle silicon dies. Test vehicles were designed to extract daisy chain resistance data using four points probe method. Silicon test chips are built with different configurations:

- Chip thicknesses (50, 100, 200 µm).
- Chip sizes (square of 2, 4, 8 mm).
- Bump size (25µm, 50µm, 65µm diameter).
- Pitches of the bumps (50, 100, 150, 250 µm).
- Number of interconnection rows (1, 2, array).
- Redistribution layer (RDL).

These configurations are designed in order to obtain a large amount of information for defining future functional SIPs. For illustration, two configurations are presented in figures 3 and 4.

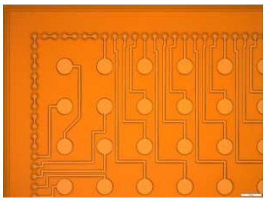

Figure 3: 4 mm RDL chip chip's with 200 µm pitch ECD.

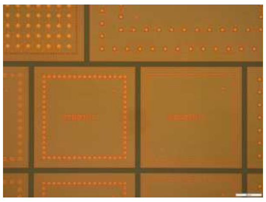

Figure 4: 2mm and 4mm before copper-pillar.

The conductor lines are made with sputtered aluminum metallization, with a mineral SiO_2/SiN passivation layer on top and a SiO_2 oxide layer underneath. This part constitutes the first routing level. These different configurations are designed with one or two rows of peripheral interconnections.

For some cases of the study, a second level of redistribution layer (RDL) is implemented. It is composed of an electrodeposited copper RDL allowing to enlarge interconnection pitch to a bumps array. To finish the RDL bricks one layer of organic passivation is added on top.

Substrates

Both organic and silicon substrates will be used for flip chip stacking.

Organic substrates are LGA type of 15mm by 15mm in size. Each LGA will allow the flip chip report of one test chip. The structure of the substrate is described in Figure 5.

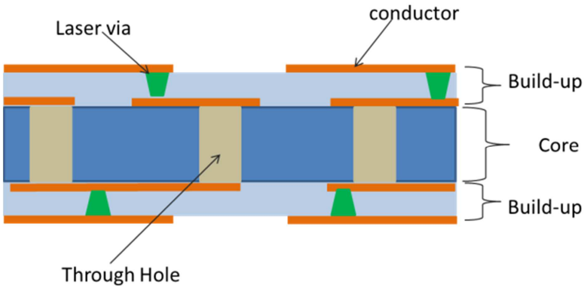

Figure 5: Representation of organic substrate section.

It is composed by a central part called core (MCL-E-679FG (R)) and two outer layers called build-up (ABF-GZ41). The total thickness is about 1mm. The layers are conventionally organized with a 1/2/1 configuration with through holes in the core and laser vias for the build-up layers. A 1mm pitch LGA pad array is present on the backside to ensure future electrical testing with a socket.

The OSP (Organic Solderability Preservative) finishing was chosen because it is considered as the most adapted for fine pitch report [16], [12]. Moreover, published studies indicate that OSP is a better choice for drop test reliability [17].

Interposer silicon substrates are used to report the chips as well. Each interposer wafer will allow the flip chip report of all the different chip configurations. The structure of the interposer is composed by the conductor lines made with sputtered aluminum metallization, with a passivation layer on top and a SiO_2 oxide layer underneath. Finishing pads are constituted of copper with SnAg solder capping. The final interposer silicon thickness is about 300µm. Standard test pads are present on each location to ensure future electrical testing with four points probe method.

Flip chip interconnections

Copper-pillar bump

Copper-pillar bumps are made at CEA LETI. The structure is composed of a copper-pillar which is manufactured by ECD (copper electrochemical deposition) on a titanium/copper/titanium seed layer. On the copper-pillar, a layer of 2 µm of nickel is grown acting as a barrier to the interdiffusion of Cu-Sn and limiting the growth of intermetallic compounds (IMC) Cu_3Sn_5 and CuSn. Subsequently, a solder 96.5Sn3.5Ag is grown to form the last part of the copper-pillar bumps. After deposition, a first reflow is carried out at 260°C to obtain a hemispherical shape of the solder as shown on the Figure 6.

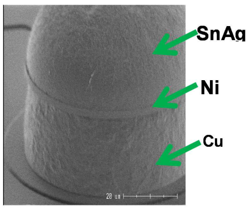

Figure 6: Copper-pillar bump.

In the study several parameters of the copper-pillar bumps will be changed. Table 1 present the different values of these parameters.

Table 1: Copper-pillar bump characteristics.

Pitch µm	all	100-150-250	100-150-250	100-150-250
Height of µpillar (µm)	20	40	60	75
Pitch (µm)	50	100	150	250
Diameter (µm)	25	50	65	65

Gold-stud bumps

Gold-stud bumps are manufactured by a modified process of wire bonding. After deposition on the pad we obtain a stud bump as shown in the Figure 7.

The height of a typical gold-stud bump is around 20µm and the diameter is around 50µm.

Gold-stud bump technology exists with pitch of 50µm [18] or less, so the pitch is not a real limitation for this process.

Secondly, the most important point is the comparison of gold-stud bump with copper-pillar on reliability performances under thermal cycling test.

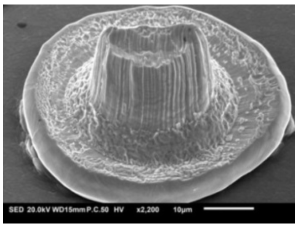

Figure 7: Gold-stud bump.

Underfill

Once the chips are assembled on the substrates, the next step is the underfilling process to fill the space between the chips and the substrate. This allows a mechanical reinforcement of the assembly that can prevent failures. The underfill provides protection against the deformation of the assembly due to the difference of coefficient of thermal expansion between the silicon (3E^{-6} /°C) and the organic substrate (17E^{-6} /°C). In addition, the underfill provides protection against the environment such as dust and moisture.

For the underfill to play totally its role, it is necessary that the dispense is made correctly. In case of the presence of voids, this could be the source of stress concentration and the start of cracks propagations.

NAMICS underfill material is used for this step.

Global reliabilities test

Figure 8 represents the overall process flow describing the study. Electrical tests are performed at different levels of the flow to control the process and finally at different stages of the stress test.

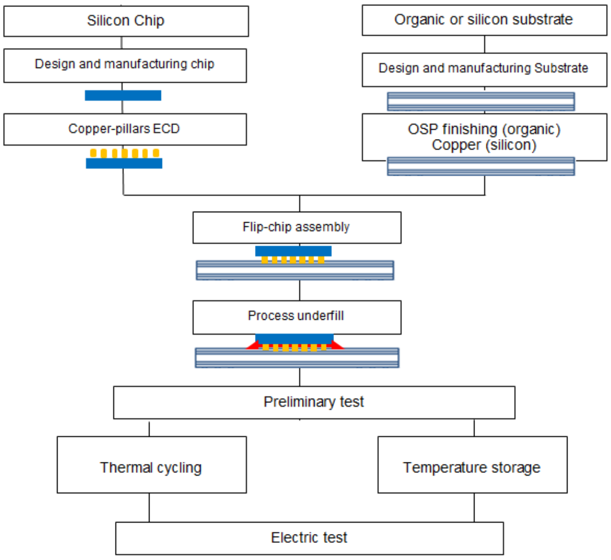

Figure 8: General process flow of the study.

As shown in Figure 8, all the test vehicle samples are checked after assembly in order to validate the interconnection integrity. On one part of the samples a storage temperature test is carried out to see the evolution of the intermetallic compounds (IMC). On a second part of the samples thermal cycling between -55 °C and 125 °C is performed in order to obtain lifetime information. For that every 200 cycle's electrical tests are done to extract daisy chain resistance data. Measurement method used is a four points to avoid contact resistance issues. Also kelvin measurement is performed on one interconnection in order to understand more precisely the bump evolution during cycling.

III. THERMOMECHANICAL ANALYSIS

FINIT ELEMENT METHOD

ANSYS program was employed to evaluate plastic strain energy of the flip-chip report. Stress is principally due to CTE mismatch between the silicon chip and the receiving substrate. Three-dimensional solid elements with eight nodes were chosen for the finite element analysis. The mesh near the copper-pillar bump is chosen smaller than the other parts, to allow a convergence of the results. Mesh used is shown on Figure 9.

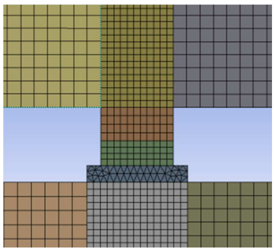

Figure 9: Mesh used for copper pillar model.

The results were obtained using Anand law (1).

$$\dot{\varepsilon}_{pl} = A e^{\left(-\frac{Q}{R\theta}\right)}\left\{\sinh\left(\xi\frac{q}{s}\right)\right\}^{\frac{1}{m}} \quad (1)$$

Equation 1: Anand law.

$\dot{\varepsilon}_{pl}$ = Equivalent plastic strain rate
A = constant with the same unit as the strain rate
Q = activation energy with unit of energy/volume
R = universal gas constant with unit of energy/volume/temperature
θ = absolute temperature
ξ = dimensionless scalar constant
s = internal state variable
m = dimensionless constant

We consider a perfect bump and a perfect contact interface with no void.

Chosen criterions are usually the per-cycle inelastic strain, called PLWK. This criterion is used to represent the behavior of solder when thermal cycling is performed on the package.

In order to have a criterion, the average of plastic strain energy (2) is used to obtain one value in each configuration:

$$\Delta W_{ave} = \frac{(\sum \Delta W \times V)}{\sum V} \quad (2)$$

Equation 2: Average plastic strain energy per cycle.

Where ΔWave is the average inelastic strain energy density accumulated per cycle, ΔW the strain energy density accumulated per cycle for each element and V the volume of each element.

In order to be realistic, tests are done to ensure having the less dependency of the mesh but keeping time of processing at reasonable value. Moreover, average plastic strain energy per cycle prevents mesh dependency due to geometrical edge effect [21], [22] . Also, law stability has to be checked and after three cycles, density energy change has to be lower than 1%.

Thermo-mechanical parameters introduced in the model are described in **Table 2: Material properties.Table 2** and **Table 3Erreur ! Source du renvoi introuvable.**.

Table 2: Material properties.

	CTE (ppm/°C)	E (Gpa)
Silicon	3	131
Organic substrate	17 28	25
Copper	17	121
SnAg 3,5	30	39

Table 3: Anand parameters for SnAg solder.

Anand parameters [19] [20]	So	R	A	ξ	m
Mpa K s-1	39,09	8900	22300	6	0,182
Anand parameters	h0	s	n	a	
Mpa K s-1	3321,2	73,81	0,018	1,82	

Elastic behavior properties are used for chip, substrate and copper. SnAg solder behavior is considered with a viscoplastic law as described in the next chapter.

Study is focused on thermal cycling reliability. The choice for the temperature excursion according to SAFRAN needs is fixed between -55 °C and +125°C.

V. Conclusion

In this paper, we present the design and the fabrication of a test vehicle having different configurations of interconnects dedicated to a reliability study of silicon die - to- substrate flip chip assembly. Chips with 2 mm, 4 mm, and 8 mm are used with several configurations of µbumps. For all those configurations organic and silicon receiving substrates have been also developed and fabricated. The focus of this work is made on copper-pillar technology but comparison will be also made with gold-stud bump interconnects. The main goal of these test vehicles is to study the behavior of the flip chip interconnects during thermal cycling between -55°C and +125°C. The final objective is to assess the reliability for each interconnect configuration. Besides, the most critical parameters acting on thermal reliability will be determined. In parallel, thermo-mechanical analysis by finite element modeling are performed to extract values of plastic strain energy per cycle and predict the failure mechanisms.

The ultimate aim of this study is to determine SIP design rules for future airborne functional assemblies.

V. Acknowledgment

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