Module Stress Reduction for 2.5D TSV-based Heterogeneous Package

Hoon Jung, Quan Pham, Bryce Lukehart, Haamid Juvale, MinKeon Lee, JunOh Bong, HyungSang Park
Amkor Technology
2045 E. Innovation Circle
Tempe, AZ 85284
480-821-5000
Hoon.jung@amkor.co.kr, Quan.Pham@amkor.com, Bryce.Lukehart@amkor.com,
Haamid.Juvale@amkor.com, MinKeon.Lee@amkor.co.kr, JunOh.Bong@amkor.co.kr,
HyungSang.Park@amkor.co.kr

Abstract

Resilience to mechanical stress is an essential requirement for successful electronics applications. This paper investigates how underfill and metal lid adhesive choice effect module stresses in 2.5D Through Silicon Via (TSV) based heterogeneous packages. Key material properties such as glass transition temperature (Tg), modulus of elasticity and coefficient of thermal expansion (CTE) are critical when package warpage is varied from room to peak (240~260°C) reflow temperatures. Application-specific integrated circuit (ASIC) die (especially in 5 nm wafer node), high-bandwidth memory (HBM) (trending toward HBM3, HBM3E and HBM4 series) as well as larger, thicker substrates are driving a sharp increase in package costs. This increase in material costs makes it difficult to perform engineering evaluations with a sufficiently high sample size. Utilizing mechanical stress simulations is a cost-effective alternative. This paper describes ANSYS module stress simulations run with both flat-top lid and stiffener ring designs of various foot widths and thicknesses. This allows for the assessment of a variety of underfill and metal lid adhesive choices in the different package configurations. Then, when a key configuration is identified, physical test vehicles can be made to confirm simulation results. Using a Chip on Wafer (CoW) assembly test vehicle with 72-mm x 72-mm package size and 39-mm x 35-mm module size, it was determined that the choice of these materials is critical, not only for package warpage management, but also for module resistance against mechanical stress in reliability testing.

Key words

Heterogeneous Integration, Package Warpage, Module Stress Simulation, Chip on Wafer (CoW), 2.5D Silicon Interposer, High-Bandwidth Memory (HBM), Underfill for Chip on Wafer (CoW)

I. Introduction

The accelerating demands of artificial intelligence (AI) and computing markets have created a push for a more complicated package structure. To meet the demand for increased processing speeds, memory location is trending towards closer and closer physical proximity to the central processing unit (CPU). This drives the adoption of the so-called 2.5D packaging technology. This involves first using a Chip on Wafer (CoW) process, then singulating the module and proceeding with traditional flip chip (FC) assembly.

There are several reasons why 2.5D packaging is preferred. In 2.5D, the main CPU and memory are connected to the package substrate with a silicon interposer, which also utilizes through silicon vias to traditional copper (Cu) pillar (CuP) interconnects with the package substrate. This silicon interposer utilizes finer lines and spaces and can reduce the distance between logic and memory to <100 µm. The shrinkage in distance can reduce signal delays, preserve signal integrity, and lower energy consumption which is key in high performance computing applications. The progression of signal path reduction is shown in Fig. 1 below. Another benefit of 2.5D packaging is the increased interconnect density that is possible over a traditional organic substrate. Current high-bandwidth memory (HBM) chips have roughly 4000 connections. The 2.5D package structure is visualized in Fig. 2 which shows the interconnections between the organic substrate and the silicon interposer.

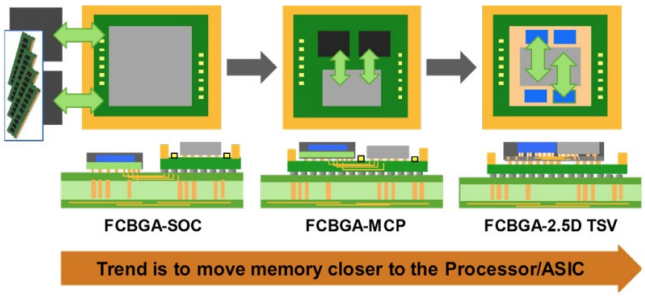

Fig. 1. *Advanced packaging trends.*

The 2.5D modules are larger than a typical monolithic die and are subject to intense thermal and mechanical stresses during thermal cycling. One of the common failure points is underfill cracking in the interface between the organic substrate and silicon interposer. This can lead to failures in C4 or CuP interconnects. To maintain yields, it is critical to choose the correct materials for underfill and lid adhesive. Key elements of the solution include the three structures shown in Fig. 2:

(1) Integration of HBM and serializer/deserializer SerDes microchips using micro-bump joining to an interposer.
(2) Through Silicon Via (TSV) interposer connections to C4 or large CuP.
(3) Package substrate.

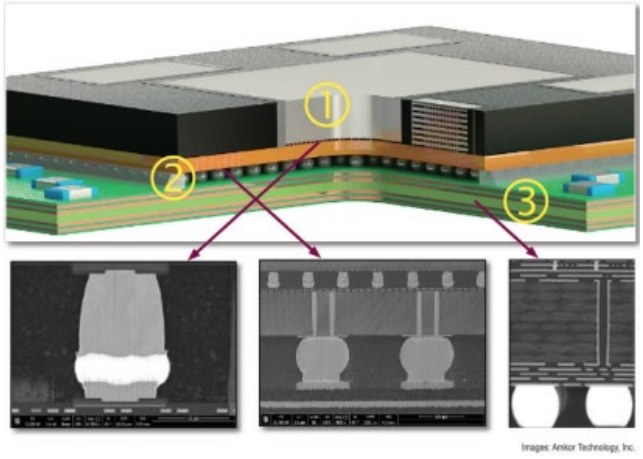

Fig. 2. *Three key elements of advanced 2.5D packaging technology.*
`

II. Experiments and simulations

A. Test vehicle information and thermal cycling

In this paper, a 2.5D package with TSV silicon interposer will be studied (see Table 1). The purpose of this test vehicle is to validate the assembly process and the reliability of the design and the selected packaging materials before committing expensive, functional components. Thus, for the validation and reliability testing, mechanical representatives with daisy-chain test nets are used in place of functional components; these are referred to as "mimic" components. Within the heterogenous integrated module are two mimic HBMs, a mimic ASIC, and dummy silicon (Si) filler die. After successful test vehicle assembly, the packages were subjected to package-level thermal cycling test, C condition (-65 to 125°C). During the inspection points, scanning acoustic tomography (SAT) imaging showed there were signs of cracking or delamination within the heterogeneous module. These units were then taken for destructive failure analysis where cross-sections confirmed the presence of underfill cracking. The crack was determined to be between the top die and the silicon interposer and at the corner of the mimic ASIC as shown in Fig. 3.

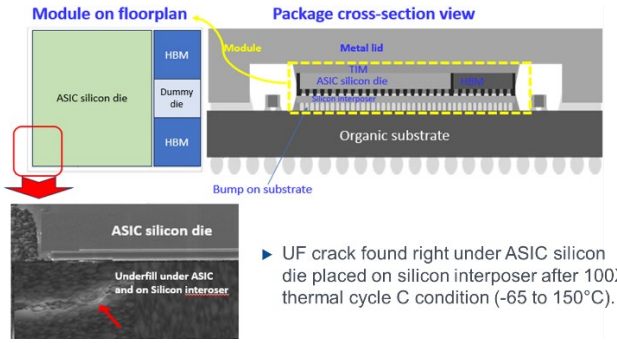

Fig. 3. *Example underfill crack in 2.5D package.*

Table I. Package Specifications.

Package size	72 x 72 mm
Logic size (mimic)	26 x 31 mm (full die thickness)
Si interposer thickness	0.1 mm
HBM size (mimic)	10 x 11 mm, HBM2 mimic
Substrate	thickness/layer/build-up/core: 2.0 mm/16 layers/ABF GZ-series/T-glass core, 1.2 mm thickness
Metal lid	71.5 x 71.5 mm size Cavity depth 0.9 mm Lid feet: 8 mm Thickness: 3 mm
Total package height	5.65 mm
Bottom ball grid array (BGA) pitch/raw ball size	1.1/0.6 mm (full grid array)

B. Finite element analysis model

Mechanical simulations were used to help determine the appropriate design and material changes that could mitigate the underfill cracking issue found during thermal cycling. A representative finite element analysis (FEA) model was built with temperature-dependent material properties. Thermal cycling stresses were simulated by applying temperature

changes to the model. These temperature changes then drive the subsequent thermal strains and stresses that arise due to the mismatches in coefficient of thermal expansion (CTE) between the different materials that comprise the package. This approach is adequate for stress trend analysis.

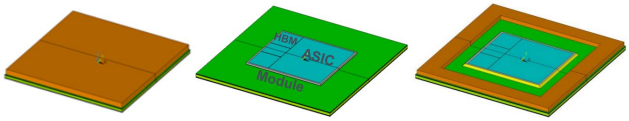

Fig. 4. *Simulation models: lidded 2.5D package (left), lid removed to see module (middle), and stiffener package version (right).*

In the model, the region of underfill that experienced cracking was closely investigated to check for stress behavior that would correlate with the reliability testing observations. A cross-section of this region and a stress contour is shown on Fig. 4. The simulation shows relatively high stress concentrated around the corner of the ASIC die which correlates well with the crack location observed. This stress output was then used to compare various package designs and materials.

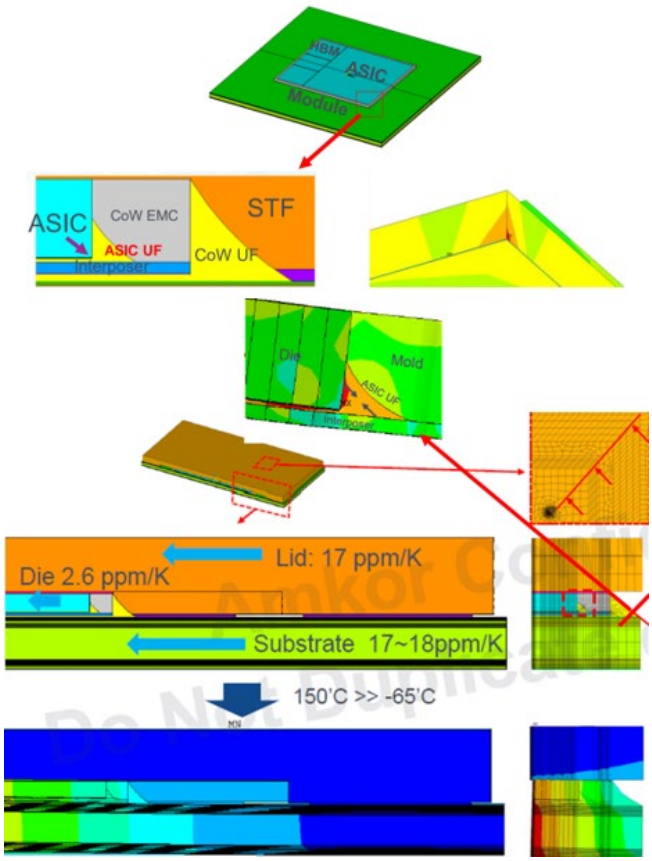

Fig. 5. *Detailed model cross section with a purple arrow showing stress contour viewing direction (left), and stress contour on ASIC underfill (right) as well as pointing the spot (ASIC die's corner, bottom) for stress simulation.*

C. Stress simulation DOE

Based on the thermal cycle failure mode, several material and package attributes were chosen to study their effect on the underfill stress magnitude:

1. Die underfill – switching a failing material to a different material is a nuanced topic: not only do the specific material properties such as modulus, CTE, and Tg influence its stress level, but the inherent strength will change from material to material which complicates the comparison. For example, fatigue resistance, toughness, yield point, tensile strength, elongation limit, temperature stability are material specific, and all play a role in the failure outcome. Nevertheless, it is still valuable to understand how stress may be influenced by switching materials. For this study, an alternative die underfill with higher Tg will be compared.

2. Lid type – the current design of the package incorporates a flat-top lid which serves many roles: to protect the heterogeneous module and package top surface, to be an integral part of the thermal path to the final thermal solution, and finally to interact with all other package materials to achieve acceptable coplanarity for subsequent assembly steps. However, by applying force onto the package through the thermal interface material (TIM) and lid foot adhesive, the lid will also impart stresses, especially at the module corners. The simulation compared the effects of switching to a stiffener ring.

3. Lid foot adhesive – the adhesive material used can play a significant role in the warpage of the package and the stress in certain regions. The modulus of the adhesive is a key attribute because it determines how well the substrate edges and the lid foot are coupled, which will maximize the interaction of the lid or stiffener with the substrate. However, the adhesive can also impart higher stresses into the die or module from increased substrate bending.

A simulation study was conducted based on the three factors discussed above. Their effects on the ASIC underfill stress are plotted in Fig. 6.

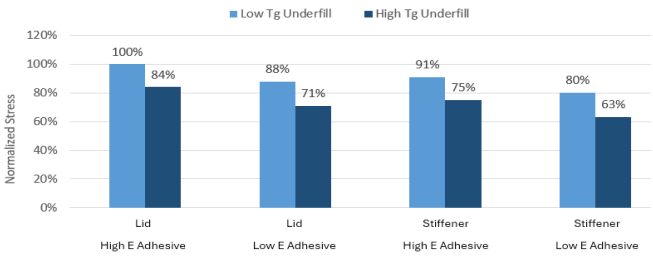

Fig. 6. *Plot of relative stress comparison.*

The results show expected trends with a reduction in stress due to the high Tg underfill, low modulus lid adhesive, and stiffener, in the order of stress reduction magnitude. The higher Tg underfill has a transition temperature significantly higher than the high temperature dwell of the thermal cycle condition. This can benefit the underfill stress because the thermal strain the occurs during each cycle is entirely comprised of CTE1, thereby reducing the overall thermal strain of the underfill. The low modulus adhesive and the switch from lid to stiffener ring had a moderate stress reduction effect as well.

D. Follow-up build and analysis

Procuring stiffeners would lead to a lengthy project delay, so it was decided to continue with test vehicle builds using the alternative die underfill material and lower modulus lid adhesive, which simulation estimated to reduce stress by 39%. These packages were successfully assembled and submitted to the same thermal cycle reliability testing as before. With the package and material changes, the test vehicle passed the reliability testing with no abnormal SAT, or underfill cracking. However, the changes that allowed the test vehicle to pass thermal cycle testing consequently increased the package warpage. The measured package warpage (shown in Fig. 7) measured from the substrate BGA-side and the 2D diagonal profiles are in dead-bug orientation. The interaction between the module and the substrate is clearly observed in the curvature at the center of the package. Then, outside of the module area, the substrate and lid interaction pulls the substrate back towards the peak or valley. As previously mentioned, this will reduce warpage but can introduce stress into the module corners.

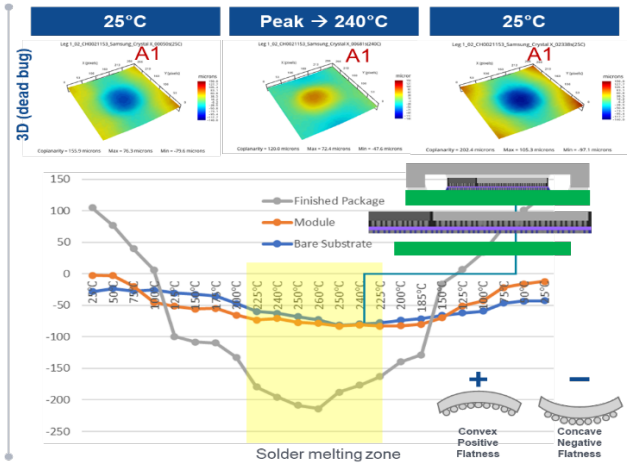

Fig. 7. *Package warpage measurements (top), package diagonal profiles: 25°C (left), 125°C (mid), and 260°C (right).*

An additional simulation study was performed to identify a design that will have low stress and low warpage. This study will investigate several additional factors such as core material, core thickness and stiffener material. The details are shown in Table II. Core material and its thickness can have a strong influence on the package warpage and stresses. Because substrates are heavily loaded with copper for routing and power or ground planes, the core helps to reduce the overall CTE of the substrate so the CTE mismatch between a silicon die or heterogeneous module is reduced.

Table II*. Follow-up Warpage and Stress Study.*

Leg	Die underfill	Core Mat'l	Core Thk	Lid/STF	Lid Adhesive
1	Low Tg	Low CTE	1.2mm	Lid	High E
2	High Tg	Low CTE	1.2mm	Lid	Low E
3	High Tg	Low CTE	1.2mm	Stiffener	High E
4	High Tg	Low CTE	1.4mm	Stiffener	High E
5	High Tg	Ultra Low CTE	1.2mm	Stiffener	High E
6	High Tg	Ultra Low CTE	1.4mm	Stiffener	High E
7	High Tg	Low CTE	1.2mm	Stiffener (SUS 430)	High E

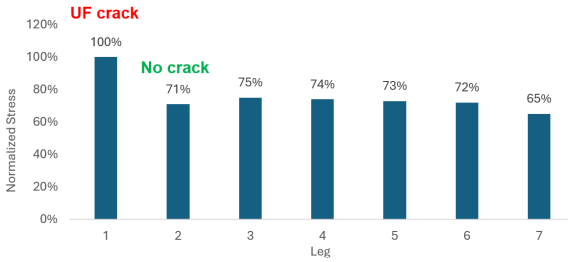

Fig. 8. *ASIC underfill stress.*

The first two legs of the simulation study reflect the known data points from the test vehicle builds so the underfill crack results are noted on the graph. The simulation results show that with high Tg die underfill material and with stiffener, the stress remains close to the known-good test vehicle design and the core material and thickness does not have a significant effect on the ASIC underfill crack. This is a promising result because there are many factors that can be selected to reduce warpage without the risk of reintroducing stress into the ASIC underfill.

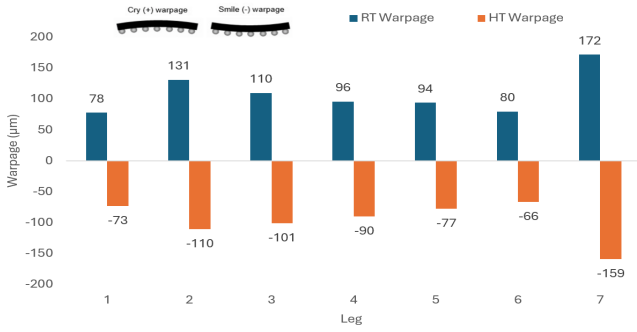

Fig. 9. *Package warpage simulation results showing Room Temperature (RT) and High Temperature (HT) warpage.*

Several key conclusions can be reached by combining the findings from the initial stress analysis in Fig. 6 with the additional results:

1. While the combination of stiffener + high modulus adhesive and lid + low modulus adhesive is roughly equal in underfill stress reduction, the resulting warpage with stiffener + high modulus adhesive is lower (leg 2 vs leg 3), meaning it has improved stress and warpage performance.

2. The effect of core CTE and core thickness is moderate, and their effects can be combined to significantly reduce warpage. As shown in Fig. 7, the package warpage is driven by the warpage within the module area. So, by reducing the CTE mismatch between the module and the substrate, this effect can be reduced.

3. In this case, the SUS 403 stiffener material was not effective in reducing warpage but was effective in reducing stress. This is likely due to the reduced CTE of the material which significantly reduces its mismatch with the substrate and consequently, its warpage-correcting abilities.

Based on the simulation results, design and material changes can be recommended for the next test vehicle builds.

III. Conclusion

As packaging trends continue towards minimizing distance between memory and ASIC die, assembly cost and complexity increase exponentially. This complexity lies not only in the manufacturing process but also in the addition of materials and interfaces within a heterogenous package. Ensuring that all the materials and their interactions can result in a reliable and warpage-controlled package is increasingly difficult, highlighting the importance of utilizing finite element analysis to determine improvement paths. In 2.5D TSV construction, failures have occurred in numerous test conditions and locations such as microbumps, TSVs, silicon interposer corner, underfill between heterogenous components. This paper discussed a case study involving die underfill cracking during thermal cycle testing of a 2.5D TSV-based package and the subsequent simulation analysis. Initial simulations were used to select design changes that successfully mitigated the underfill cracking. However, these design changes led to increased warpage, necessitating a follow up simulation study. Finally, design and material factors were identified that could both reduce underfill stress and reduce package warpage. These findings highlight the importance of using experimental data along with simulation analysis to help select the proper materials to reduce mechanical stress while still maintaining acceptable warpage levels in the package.

References

[1] Mike Kelly, “Amkor Heterogeneous IC Packaging: Optimizing Performance and Cost,” published on September 22, 2022 in Semiconductor Story https://amkor.com/blog/heterogeneous-ic-packaging-optimizing-performance-and-cost/ .

[2] “2.5D MCM (Multi-chip Module) Technology Development for Advanced Package,” 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC) https://conferences.computer.org/ectc/pdfs/ECTC2023-1NkkviSxgDnmPjptC1ysqm/349800a778/349800a778.pdf.

[3] “2.5D-Level Packaging Technology Materials, Assembly, Process, and Reliability Challenges,” Jun 14, 2022, NASA Electronic Parts and Packaging Program https://nepp.nasa.gov/docs/etw/2022/14-JUN-TUE/1255-Suh-CL-22-3179.pdf.

[4] John H. Lau, “State-of-the-Art in Chiplets Horizontal Communications,” 2023 Journal of Microelectronics and Electronic Packaging https://imapsjmep.org/api/v1/articles/81977-state-of-the-art-in-chiplets-horizontal-communications.pdf .