

A Novel High Resolution Dry Film Photo-Imageable Dielectric for Redistribution Layer in Advanced Packaging Applications

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Abstract

To meet the needs for finer pitch redistribution layer (RDL) designs on organic, glass and silicon interposers, substrates, and panels, a photoimageable dielectric (PID) dry film (DF) has been developed suitable for embedded trace dual damascene processes. This high-resolution, dry film PID is based on the aqueous developable benzocyclobutene (AD-BCB) platform already used in HVM production for redistribution layer patterning in advanced packaging. The PID is negative tone, tetramethylammonium hydroxide (TMAH) developable with a Dk of <2.9 and cure temperature of 220°C. Dry film rolls have been successfully made at pilot scale with film thickness ranging from 5µm to 45µm and is able to achieve a 2:1 aspect ratio for 10µm and 20µm films. Patterning has been demonstrated on i-line stepper, mask aligner and laser direct imaging (LDI) tools. Using a 2-stage vacuum laminator, this PID achieves excellent planarity over plated metal contacts and lines. Cured films have passed bias HAST testing (130°C, 85% RH, 96hr, 5V) with line space patterning of 13 µm and 9 µm with no delamination or copper dendrite formation. Two-layer lithography, reactive ion etch (RIE) surface treatment and the Ti/Cu sputter process have been optimized to achieve high resolution patterning with copper peel strength of ≥0.4kgf/cm after HAST (130°C, 85% RH, 96hr) for a 25µm electroplated copper layer. Moreover, the cured dry film has low shrinkage during cure, robust chemical resistance and no leaching in copper plating baths. Based on these attributes, the material demonstrates suitability for 2.5D and 3D advanced heterogeneous chiplet integration schemes including Fan-Out Wafer and Panel Level processing (FO-WLP, FO-PLP).

Key words

Advanced packaging, Benzocyclobutene (BCB), CYCLOTENE™ 6800 dry film photoimageable dielectric material, Embedded trace, PFAS free, Redistribution layer, Ti/Cu peel strength

I. Introduction

CYCLOTENE DF6800 dry film photoimageable dielectric material was developed by DuPont to meet the needs of advanced packing applications such as redistribution layers on interposers, substrates, panels and wafers. A similar platform is also being developed for waveguide applications. This paper will describe the dry film's platform and review the various process optimizations required to make a robust and functional product. DF6800 is also PFAS free which is becoming a key requirement for sustainability as the industry tries to phase out or reduce these chemicals [1]-[2].

Based on the aqueous developable benzocyclobutene platform which is used in several commercial DuPont products, this dry film product was formulated to achieve a

Dk of <2.9. With the need of lower cure temperatures for advanced packaging integration, this product can be hard cured as low as 220°C under a low oxygen atmosphere such as nitrogen. Desirable film properties include high resolution lithography, compatibility with industry standard 2.38wt% TMAH developer, high glass transition temperature (Tg), thermal stability (Td), low shrinkage and low copper migration. Patterning with polyethylene terephthalate (PET) film on the dry film PID has been demonstrated. Improving via and trench resolution by running a focus-exposure matrix was key to determine ideal dose and focus offset. PET on patterning is necessary for substrate or interposer layers where both sides are laminated and exposed to protect the side against the exposure tool chuck from scratches or contamination.

In order to build a 2 layer dielectric/1 layer metal test coupon, the first requirement was a high peel strength value of $\geq 0.4\text{kgf/cm}$ (footer), after HAST conditions. By optimizing a two-step RIE plasma process, high peel strength was achieved. After reviewing the dry film's properties and process conditions, the test coupon build will be described. Once assembled, the test coupon survived the pressure cooker test (PCT) at 121°C , 100% RH, 2atm, 48hrs followed by a 5x solder reflow at 260°C on a belt furnace. No delamination or cracking was observed optically and after X-SEM by ion milling.

II. Background

Aqueous developable benzocyclobutene was first developed by Dow Chemical Company in the early 2000's [3]. It has continued to be used by DuPont following their merger and separation into three companies.

DF6800 dry film photoimageable dielectric material is negative tone, 2.38wt% TMAH developable and available in rolls with a film thickness of $5\mu\text{m}$ to $45\mu\text{m}$. Developer contrast is achieved by incorporating reactive crosslinkers (X-linkers) into the film and using a photo initiator in a negative tone fashion. During the later thermal cure process, the BCB polymer builds molecular weight through the benzocyclobutene and olefin groups on the polymeric resin.

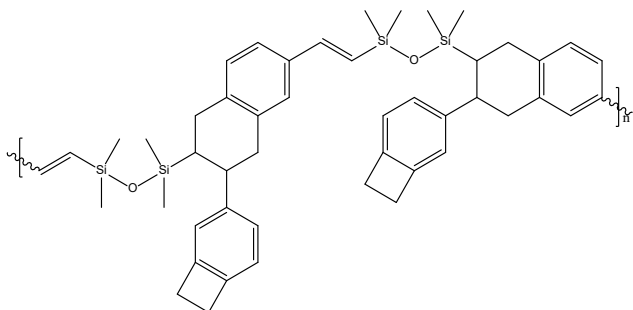


Fig. 1 (Generic structure of the BCB resin)

Once formulated, the lacquer is slot-die coated onto a polyethylene terephthalate (PET) substrate. It then goes through a series of dryers to remove the solvent before the film is protected by a polyethylene cover sheet and rolled onto a core for later use.

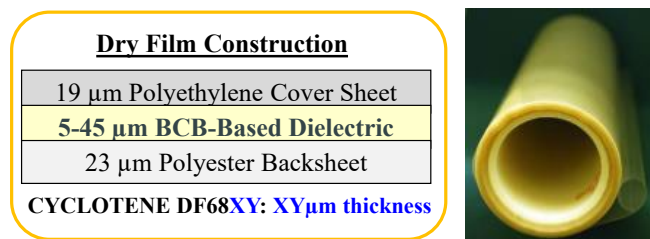


Fig. 2 (Construction of the dry film PID roll)

III. Experimental

Dry film was laminated onto a substrate such as a silicon wafer or copper clad laminate (CCL) by hot roll or vacuum lamination. The latter is preferred for improved two-layer PID adhesion, planarization and gap filling especially if using a two-stage laminator. When processing on silicon, oxide, nitride, etc., it is first recommended to prime the substrates with DuPont's AP9000C adhesion promoter to eliminate pattern undercut or lifting during TMAH develop.

A Meiki two-stage vacuum laminator was mostly used for laminating the dry films onto the various substrates. Temperatures between 110°C and 120°C with times from 30s to 60s and pressures from 0.5MPa to 1MPa are recommended to achieve the best adhesion and planarity. Thicker films are more prone to bleed out and may require processing at the lower end of the temperature and pressure range.

Exposures were done on either an ASML PAS5500/200 i-line stepper (0.48NA), Liteq 500 stepper (0.128NA), Suss MA12 mask aligner or a Heidelberg laser direct write for single layer imaging. Two-layer imaging was done on the ASML or Suss. Patterning with PET on was compared to PET off using the ASML, Suss and Liteq.

2.38wt% TMAH was the developer using a puddle process for 25-45 seconds followed by DI water rinse and spin dry.

Curing was done in a Blue M oven under nitrogen flow with oxygen levels $<100\text{ppm}$. The oven was purged followed by a 5°C/min ramp to 200°C (soft cure) or 220°C (hard cure) and held for 60 minutes before cooling at 5°C/min .

A two-step reactive ion plasma etch was done using O_2 and CF_4 gasses as a descum as well as to surface activate the film prior to PVD Ti and Cu deposition. Oxygen and a fluorinated gas such as CF_4 is required to etch BCB based materials to avoid the formation of silica on the surface which will result in poor adhesion of the next layer. Following the first etch step, a short, $\leq 20\text{s}$ O_2 only second etch step was added. It is hypothesized the second O_2 only etch step removes surface fluorination. Previous published studies have used sputtered Ti/Cu as the seed/barrier layer [4]-[7]. Plasma surface treatment at DuPont was performed using a PlasmaTherm 790+ RIE. A custom modified PECVD was used for RIE at the University of Pennsylvania. An Oxford RIE was used at Stanford University.

Etch process step 1				Etch process step 2			
CF4/O2 (sccm)	Pressure (mTorr)	Power (watts)	Time (sec)	O2 (sccm)	Pressure (mTorr)	Power (watts)	Time (sec)
75/75	85	200	20	75 O2	85	200	10

Table 1 (Example two-step etch process)

50nm Ti followed by 150nm Cu was deposited by sputter PVD. A Denton Explorer 14 was used at the University of Pennsylvania and Lesker at Stanford University. Achieving the peel strength target of $\geq 0.4\text{kgf/cm}$ required sufficient degas time to remove surface moisture. After this, a short argon plasma surface treatment was used to remove any potential surface contamination that formed between the RIE two-step plasma and PVD metallization.

Sequential Sputter Process			
	Bias	Ti	Cu
Power	100 W	350 W	400 W
Pressure	10 mTorr	3 mTorr	3 mTorr
Dep Time	60s	250s	441s
Dep Rate	n/a	2.0 Å/s	3.4 Å/s
Gas Type	Ar	Ar	Ar
Gas Flow	PID ~140 sccm	PID ~35 sccm	PID ~35 sccm
Pre-Sputter Time	n/a	300s	60s
PS Type	DC	DC	DC
Cathode	n/a	2	3

Table 2 (Conditions used on Denton Explorer 14)

After PVD Ti/Cu, the film stack was annealed at $140^\circ\text{C}/60\text{min.}$ and cooled before electroplating $25\mu\text{m}$ of copper. This was then followed by the same annealing treatment. The metal film stack was scored and 90° peeled using an Instron. Peels were done at several stages; Soft cure \rightarrow peel, then hard cure \rightarrow peel, then HAST \rightarrow peel OR hard cure \rightarrow peel, then HAST \rightarrow peel.



Fig. 3 (Example of pre and post Cu peels on DF6810 PID)

The 2 layer dielectric/1 layer metal test coupon was prepared with the following sequence.

1. Lamination of DF6800 on AP9000C primed silicon
2. Via patterning
3. $220^\circ\text{C}/60\text{min.}$ hard cure
4. RIE plasma surface treatment
5. PVD Ti/Cu followed by anneal

6. Electroplated Cu followed by anneal
7. Chemical mechanical polishing
8. RIE plasma surface treatment
9. 2nd layer DF6800 lamination
10. $220^\circ\text{C}/60\text{min.}$ hard cure

Once the test coupon build was completed, it underwent PCT followed by 5x reflow. The coupon was then optically inspected for delamination or cracking, and ion milled for cross-sectional SEM.

IV. Results

Various lithographic, mechanical, and electrical properties were collected on DF6800 laminated and cured films.

Property	DF6800
Film Thickness	$5\mu\text{m}$ through $45\mu\text{m}$
Exposure Dose	$75\text{--}150\text{ mJ/cm}^2$ for thinner films
Develop Time (for $15\mu\text{m}$ film)	45s Single Puddle (DF6815)
Aspect Ratio	2:1 (1.25:1 for $5\mu\text{m}$)
Shrinkage (cure)	5.2%
Tg	$>250^\circ\text{C}$
CTE	$67.5\text{ ppm/}^\circ\text{C}$
Residual Stress	30 Mpa
Modulus	2.7 Gpa
Elongation	10% avg (15% max)
Tensile Strength at break	90 Mpa
Moisture Uptake	0.84%
Thermal Stability	359°C for 5% wt loss
Dielectric Constant @ 10 GHz	2.87
Dissipation Factor @ 10 GHz	0.019

Table 3 (Film properties of DF6800 PID)

To demonstrate the gap fill and planarization of dry film, the first layer was patterned and soft cured. To enhance contrast, the first layer was then sputtered with Ti/Cu before laminating the second layer using a 2-stage vacuum laminator. After the final hard cure, no voids were seen in the patterned first layer. Neither were dimples seen the second layer indicating excellent planarization.

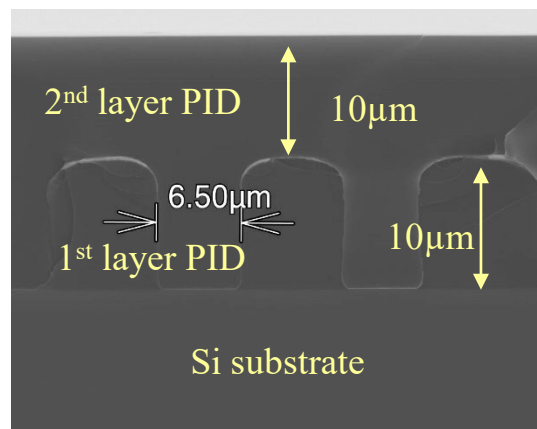


Fig. 4 (Via filling and planarization of first layer)

To further push the gap filling properties, DF6820 was laminated on a nominal 400 μ m deep by 45 μ m wide trench in silicon. No voiding was observed with complete trench fill.

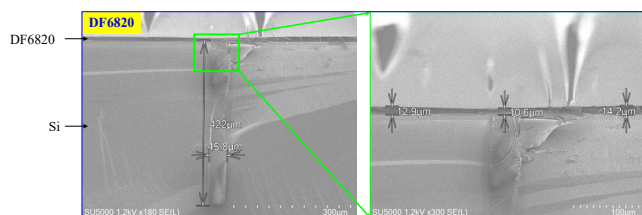


Fig. 5 (Gap filling of 400 μ m deep trench in silicon)

Single layer dry film was successfully patterned with multiple tool sets at various film thickness. The PID was able to pattern 6 μ m trenches with >2:1 aspect ratio using a 0.48 NA i-line stepper.

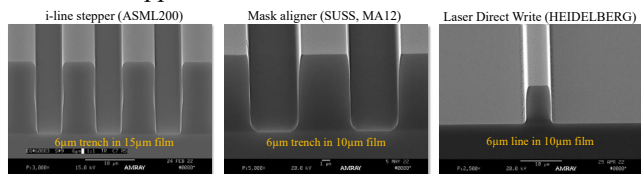


Fig. 6 (Single layer patterning with exposure tools)

Another important property is having a large process window with respect to exposure dose. With the shorter 25s develop time, the via closes up at over-exposure. In contrast, a 45s develop time enables a wider process window at over-exposure.

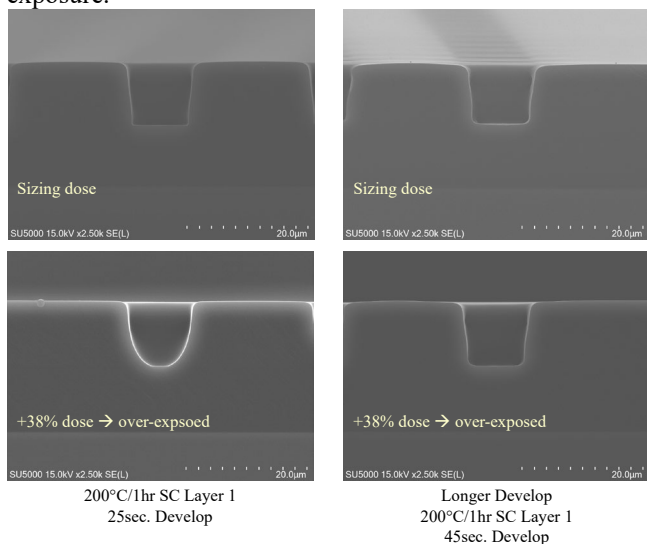


Fig. 7 (Develop time effect on resolution at over-exposure)

Single layer patterning without PET is acceptable for wafer level processing (single side processing). However, double sided processing is typically performed for panel level applications. Double sided substrates require exposing with PET on to avoid scratches or contamination of the bottom

layer of PID. After both sides are exposed, the PET is immediately removed and then developed.

Wafer level processing

PID Film
Wafer

Panel level processing

23 μ m PET substrate
PID Film
Substrate
PID Film
23 μ m PET substrate

Fig. 8 (Comparison of single and double sided film stack)

Patterning with PET on required re-centering focus offset, where tool dependent, and exposure dose to enable a large process window. For exposure tools such as a stepper, the focus offset will shift relative to PET off because of the additional film thickness. For the ASML 200 and Liteq 500 steppers, the focus offset increased by 12 μ m. Exposing through PET also results in ~15% faster photospeed.

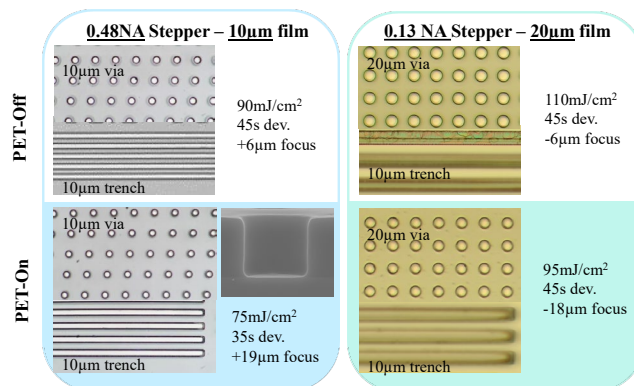


Fig. 9 (DF6800 PID film patterned with PET off/on)

In addition to fine line patterning, achieving good adhesion between PID and plated Ti/Cu assessed by high peel strength of ≥ 0.4 kgf/cm post HAST is necessary for PID. Through the two-step plasma process, sufficient degassing and argon plasma preclean prior to sputtering Ti/Cu, peel strength was increased from ~0.05 to ≥ 0.4 kgf/cm, post HAST. Subsequent peel rounds confirmed the improved peel strength post HAST.

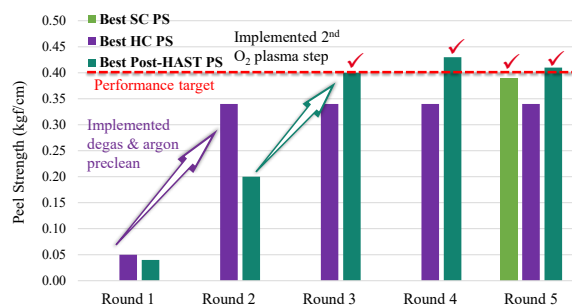


Fig. 10 (Improving Cu peel strength on DF6810 PID)

Using XPS depth profiling, differences in the Ti layer composition were seen between low and high peel strength post HAST. Oxidation of the Ti layer correlated with low peel strength whereas almost no oxidation correlated with high peel strength.

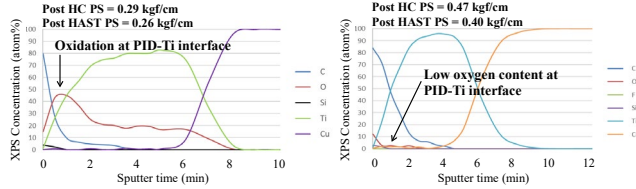


Fig. 11 (XPS depth profiling of Ti/Cu layers)

Before constructing a test coupon, the dielectric's resistance to copper diffusion had to be demonstrated. For this test, DF6815 was laminated and cured onto a comb structure of copper lines at different widths/spaces. The film stack was subjected to 5V bias under HAST conditions for 96 hours. Neither change in resistivity was detected nor was there any indication of copper dendrite formation.

Dielectric	Cu Line/Space (μm)	Resistance		bHAST 130°C/85%RH/ 96hrs	Bias	Result
		Before HAST	After 96hrs HAST			
DF6815	30/100	>10 ¹² Ω	>10 ¹² Ω	No dendrites	5V	PASS
DF6815	13/9	>10 ¹² Ω	>10 ¹² Ω	No dendrites	5V	PASS

Table 4 (bHAST results of DF6815 PID)



Fig. 12 (Copper lines/dielectric spaces post bHAST)

Following the successful bHAST test, a 2 layer dielectric/1 layer metal test coupon could be built as outlined in the experimental section.

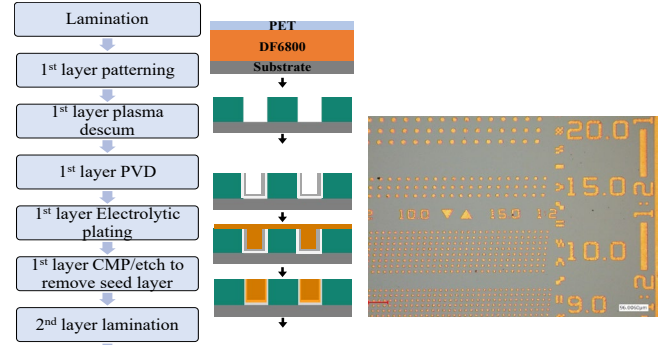


Fig. 13 (Process flow and topdown image of the test coupon)

The coupon was subjected to PCT followed by 5x reflow at 260°C/30s. The oven zones were defined using the IPC/JEDEC J-STD-202 revision C standard. After cooling, no cracking or delamination was observed under optical microscope inspection. The coupon was then ion milled for cross-sectional SEM. Once again, no indication of cracking in the dielectric or delamination at the metal interfaces were observed.

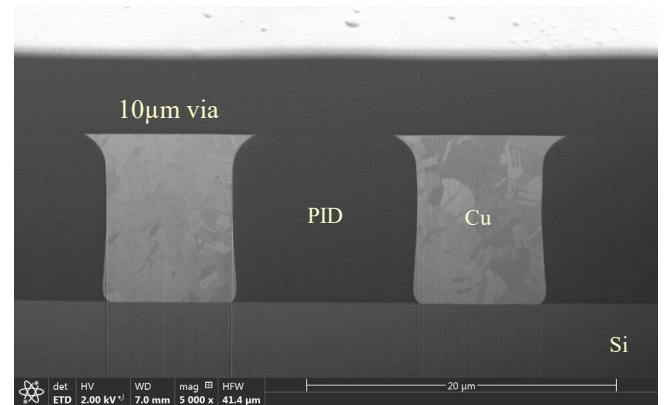


Fig. 14 (SEM image of the test coupon post PCT/reflow)

V. Conclusion

CYCLOTENE DF6800 photoimageable dielectric material developed by DuPont passed 2 layer dielectric/1 layer metal coupon reliability testing. After PCT and 5x solder reflow, no delamination or cracking was observed. During product development, many challenges were overcome such as optimizing the RIE surface treatment to achieve $\geq 0.4\text{kgf/cm}$ peel strength, post HAST. The 2.38wt% TMAH develop process was adjusted to maximize the process window of a 2 layer PID film stack. The cured dielectric passed bHAST testing with no change in resistivity or evidence of copper migration. This dry film PID is currently being sampled for RDL, embedded trace and waveguide applications.

Next steps will be fabricating a ≥ 2 layer dielectric/metal daisy chain electrical test vehicle for temperature cycle testing (TCT) along with HAST and solder reflow.

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