Using FEM Simulation to Predict the Mechanical and Thermal Performance of FO-EB-T Package

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Abstract

In order to solve the problems that high price and low process yield of single multi-functional large-size chip, homogeneous and heterogeneous integration has become the trend of modern high-end packaging technology due to faster signal transmission speed and also a benefit for space management. According to that, the development of chiplet advanced packaging technology is particularly important. During the chiplet packaging process, many structural mechanical warping problems may be encountered. In addition to the difficulty of the process, the accompanying challenges also have more severe thermal problems. Take server for example, The Thermal Design Power (TDP) of the server is increasing year by year. It can basically reach more than 500W per package. Above that, before the overall packaging is completed, the reliability issue and thermal problem must also be taken into consideration. So the selection and matching of packaging materials need to be carefully selected, including organic interposer, heat sink, adhesive, etc.

The Fan-Out Embedded Bridge with TSV (FO-EB-T) structure is taken to be the test vehicle in this paper. The assembly process of chiplet integration is firstly studied for wafer warpage in silicon bridge die with TSV connection process, pre-molding, u-pad, die bonding, underfill, molding process and C4 bump process. The glass carrier and organic compound candidates are predicted to make the wafer warpage within the criteria of each process and also show good alignment with experimental data. Simultaneously, the package warpage investigation is checked by the best combination of organic compound selection. Finally, the overall reliability and thermal performance is simulated through structure and material parametric simulation such as heat sink type and core type.

Overall, this paper proposes the simulation method to predict both in-process warpage and reliability stress performance and also take thermal performance into considered. Besides, the metrology of in-process warpage prediction will be explained which suffers the saddle shape warping performance. Above that, the FO-EB-T package development that can save the DOE and reduce the warpage and stress risk is been proposed.

Key words

High-end Package, chiplet, FO-EB-T, wafer warpage, reliability, Thermal behavior

I. Introduction

Homogeneous and heterogeneous chiplet packages were solution to the demands of high-end products, such as artificial intelligence (AI), high performance computing (HPC) processor, etc. Normally, the Chip-on-Wafer-on-Substrate (CoWoS) package are widely used to achieve the high transmission rate. But recently, the package size and chip module size have become larger and larger due to the function complexity. The problem of low yield of silicon interposer also occurred. In order to deal with the low yield problem of silicon interposer, the organic interposer which is used in Fan-Out Embedded Bridge with TSV (FO-EB-T) package is springing up to replace the silicon interposer due to its high degree of process flexibility and even low cost [1].

FO-EB-T package had been studied in many studies. The evaluation and measurement for the electrical performance

has been pointed out in research [2]. Compared to the normal FO-EB package, the power delivering performance for FO-EB-T can improve about 50%. Before the chip module singulation, the process wafer warpage control is particularly important that is limited by machine handling capability. Compared to the CoWoS chip module, the FO-EB-T chip module basically combined with two organic compounds and silicon as the main structure. During controlling the warpage of wafer, the combination of two organic compounds is always used as the control factor by coefficient of thermal expansion (CTE) mis-match effect. In research [3], the DOE matrix with compound combination has been studied to perform the smaller CTE mis-match to engage the optimized wafer warpage and chip module warpage.

After the chip module bonding process, the next focus should be on the package warpage, reliability and also thermal performance. In the publication [4], the package warpage and reliability stress performance has been studied. Using low CTE substrate core material and thicker heat sink not only can reduce the package warpage but also reduce the compound crack risk. For the thermal management, the publication [5] presented the FO-EB package thermal performance DOE matrix under system level cooling and pointed out the main factor that influence the FO-EB package thermal performance in system level cooling condition. But in the package level, it shows about 10% difference while using the liquid metal thermal interface material (TIM) with forged type heat sink except for the ring type heat sink that directly exposed the top die.

Above all, before the real product come out, the in-process mechanic warpage, package warpage, reliability and thermal performance all have important role. This paper is firstly using simulation to find out the proper compound candidates and matching to ensure the wafer warpage is within the machine handing limitation, then the DOE matrix will be purposed to find out the sweet spot that can meet the package warpage, reliability and thermal performance. The simulation software ANSYS for finite element analysis (FEA) is applied to do the warpage and reliability in this research. Thermal model is constructed by the computational fluid dynamics (CFD) analysis using the FloTHERM.

II. Structure and Modeling Information

A. FO-EB vs. FO-EB-T

As mentioned in introduction, the FO-EB package is created to be an alternative plan to deal with the yield problem of CoWoS. The connection between top die is all through the embedded die. Moreover, the FO-EB-T package further improves the electrical performance of normal FO-EB. The difference between normal FO-EB and FO-EB-T is that the embedded die contains the Through-Silicon Via (TSV) as shown in Fig 1. The signal can directly transport to substrate through embedded die with TSV. On the other hand, the chiplet process is nearly the same as normal FO-EB except the embedded die preparation process which has less risk of mechanical warping problem.

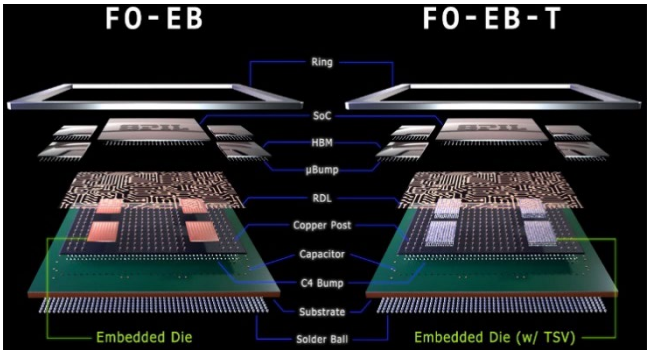
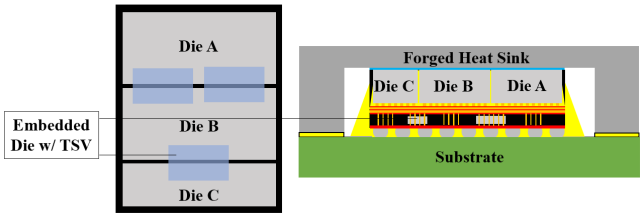


Fig 1. Comparison of normal FO-EB and FO-EB-T [3]

B. Test Vehicle Information

The FO-EB-T chip module that we applied in this research contains three top die connected with three embedded dies as a series as show in Fig 2(a). Top die A size is as same as die B, and die C is a little bit smaller. The chip module consists with 2L RDL between top die and embedded die. The package size is set as ~5000mm^2 which constructured with forged type heat sink as Fig 2(b). The rest information of this test vehicle is shown in Table I.



(a)Chip Module (b)Package w/ Forged Heat Sink
Fig 2. FO-EB-T Test Vehicle

Table I. Structure Information

Item	Size	Unit
Package	~5,000	mm^2
Chip module	~1,200	mm^2
Top die thickness	~700	um
EB die thickness	~50	um
Die gap	~150	um
Substrate thickness	~2.0	mm
Heat sink thickness	1	mm

C. *Simulation Modeling*

The simulation model is generating by ANSYS mechanical which uses FEA to calculate the wafer warpage. In wafer form simulation model, it contains 40 chip modules which are separated by the scribe line and filled up with dummy die around the chip module as shown in Fig 3. The model used to calculate the package warpage and reliability performance is shown in Fig. 4.

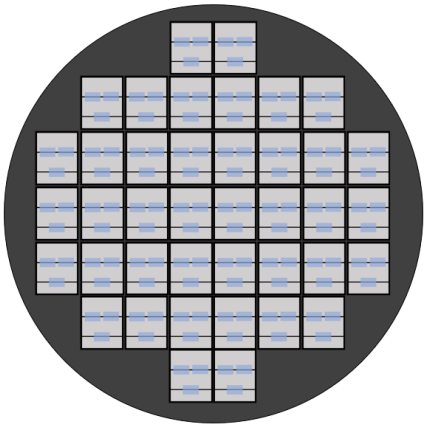


Fig 3. Wafer Model

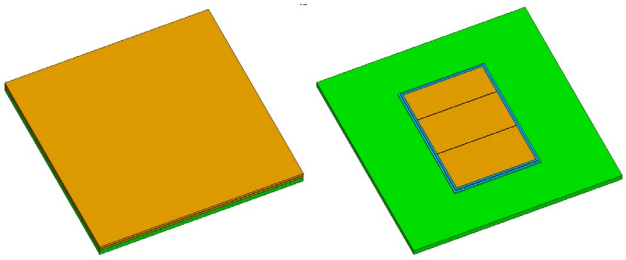


Fig 4. Package Model w/ and w/o Heat Sink

III. Simulation Results

A. *Wafer Warpage*

The process flow of FO-EB-T is shown in Fig 5. The Cu stud and embedded die is attached to the bottom PI onto the glass carrier at first. Through 1st molding process, the compound volume on top of the embedded die need to be grinded to expose the Cu stud after the molding fully cured, and begin the RDL process. In this case, 2 layers RDL is applied on the embedded die. After the RDL layer is done, the top die will be attached on the RDL layer through die-bonding process. Next, the underfill is dispensed in die gap and cured. Followed by the 2nd molding compound curing process. Then, the C4 bumps were platted on wafer after removing the bottom glass carrier. Finally, the chip module was cut out and attached to the substrate using normal flip chip process. The final package appearance is shown in Fig 5(f) after the heat sink clamping process.

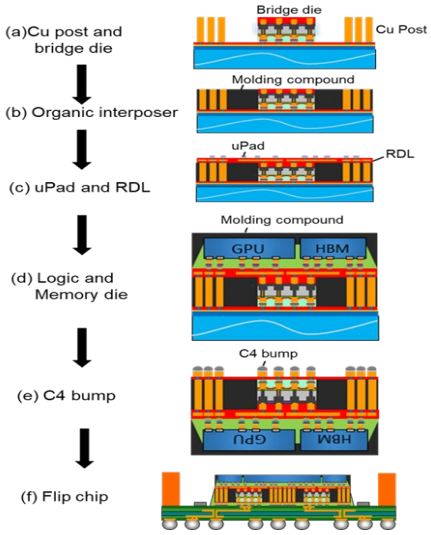


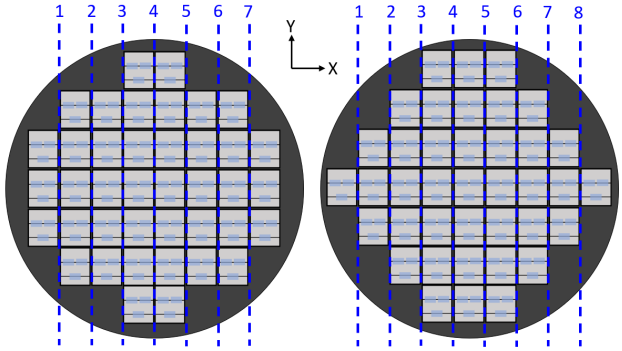
Fig 5. FO-EB-T Process Flow

In this research, there are three kinds of compound to be combined to reach the lowest warpage. The simulation DOE and material properties are as detailed in Table II.

Table II. EMC Material Properties and Combination

DOE	Pre-mold	MD1	EMC CTE
1	Type A	Type B	Type A < B < C
2	Type A	Type C	

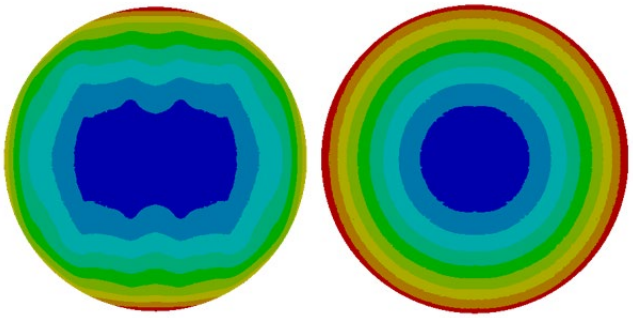
Before the best combination of these three compounds comes out, the problem had occurred after the 2nd molding process. The saddle warpage shape had emerged which can impact the machine handling capability seriously. In order to deal with this problem, we try to modify the wafer map arrangement as shown in Fig 6. The reason why the saddle warpage appeared is the series connection of top die of the chip module. The rigidity along the Y-axis is evidently lower than the X-axis. In Fig 6(a), we can see that the chip module gap count along the X-axis is 7. After the modification, the gap count is increased to 8 as Fig 6(b).



(a) (b)

Fig 6. Wafer Map Modification

Even if we can't optimize the warpage shape to the complete bowl shape, the improvement is enough to avoid the machine handling problem. The simulation contour before and after modification are shown in Fig 7.



(a) (b)

Fig 7. Wafer Warpage Contour

After solving the saddle warpage, the best combination of compounds is simulated using the new wafer map and the simulation results is shown in Fig 8. We can see that the combination of compound A and B results in lower warpage than compound A and C due to less CTE mis-match effect. And the simulation results show good alignment with the measurement results.

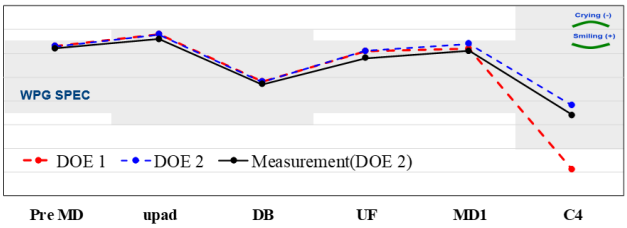


Fig 8. Wafer Warpage Simulation Results

B. Package Warpage, Reliability and Thermal Behavior

After the best compound combination is determined, the package warpage simulation is presented to judge if the warpage is out of criteria or not. In the meantime, the stress performance is also checked by the simulation. According to previous FO-EB experience, the crack will occur at the die corner at chip module top surface during the thermal cycle test as Fig 9.

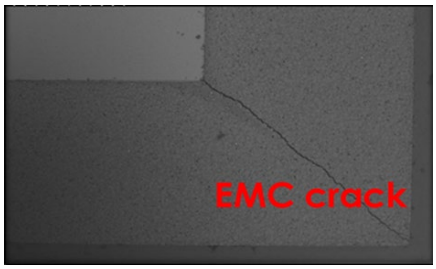


Fig 9. EMC Crack [4]

The package warpage and stress simulation results are shown in Fig 10 which follow the DOE matrix in Table III. The results show that DOE2-2 has lower package warpage and stress than DOE2-1 since low CTE core and ring type heat sink is applied.

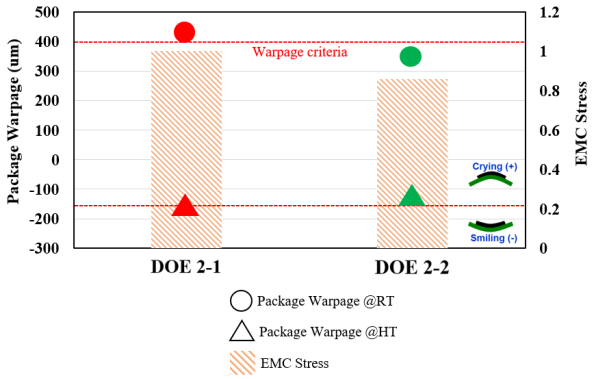


Fig 10.

Table III,

Factor	DOE 2-1	DOE 2-2
Core material	Normal CTE	Low CTE
Heat sink type	Forged	Ring

The thermal performance is finally checked by the heat flow simulation. The results show that DOE2-2 provides lower junction temperature at system level due to exposed die structure. The heat will directly dissipate by the top surface of chip module. The result is shown in Fig 11.

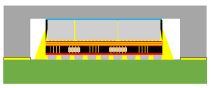
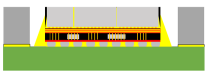
DOE	2-1	2-2
Package		
Junction temp. (°C)	103.5	91.3

Fig 11. Thermal Performance Comparison

IV. Conclusion

In this research, the best compound combination is firstly simulated. The saddle wafer warpage is been avoid through wafer map arrangement. Then, the package warpage and stress simulation results which are improved by changing to low CTE core and ring type heat sink to avoid large warpage and stress are proposed. Finally, the thermal performance is also checked to ensure the system level cooling capability.

Through simulation, the study offers the solution of high warpage and stress of FO-EB-T structure. Based on that, DOE can be saved and warpage and reliability risk reduced, and also help FO-EB-T package development in future.

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