IMAPS- INTERNATIONAL CONFERENCE AND EXHIBITION ON DEVICE PACKAGING 2024

Applications of White Light Interferometry in Advanced Packaging: Metrology and Quality Assurance

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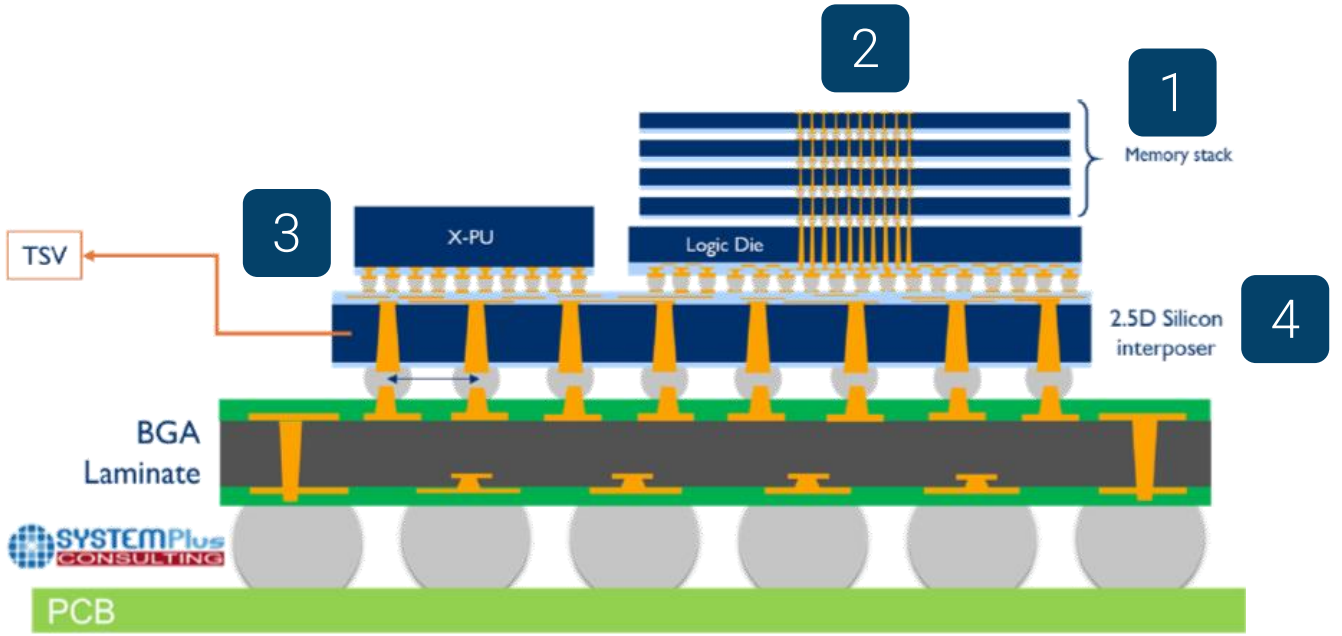
Outline

- How White Light Interferometer profiler helps:
  - Monitoring
  - Controlling
  - Optimizing

Advanced Packaging

- Outline:
  1. Die/Wafer stacking optimization
  2. Through Silicon Via control
  3. Bump control
  4. Redistribution Layer quality



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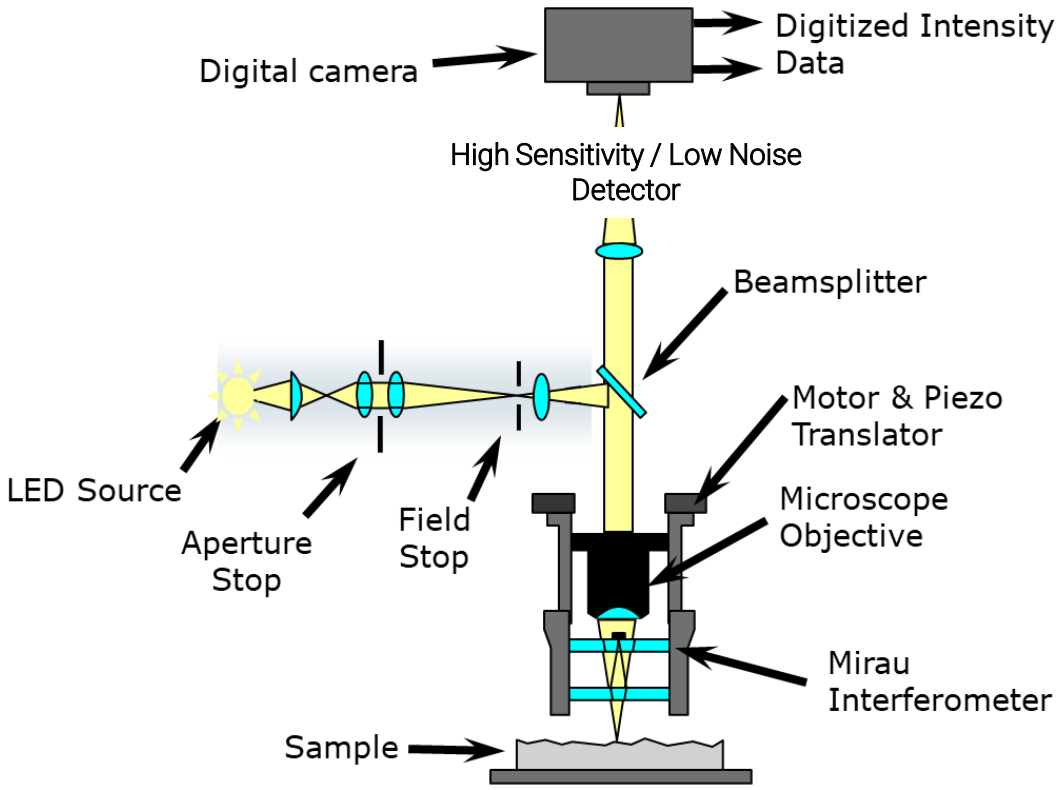
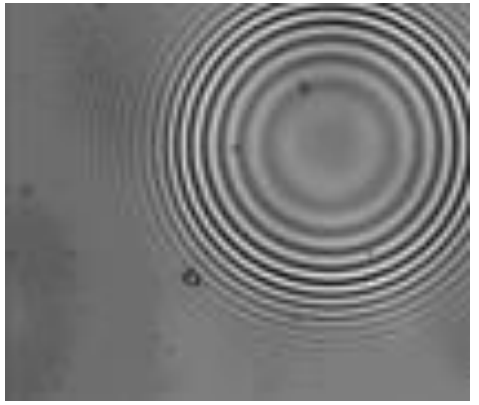
Introduction

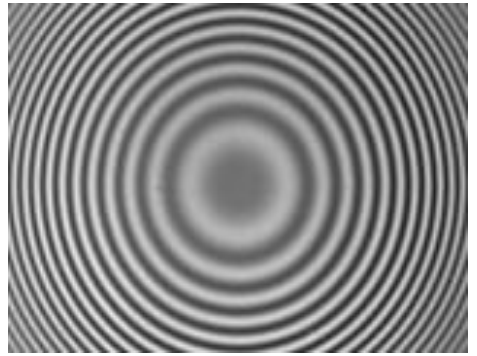
White-Light Interferometry – Key Components



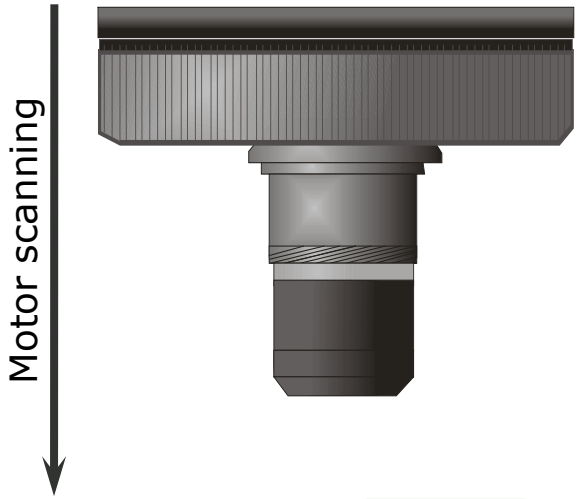
Broad Wavelength White illumination



Monochromatic Illumination



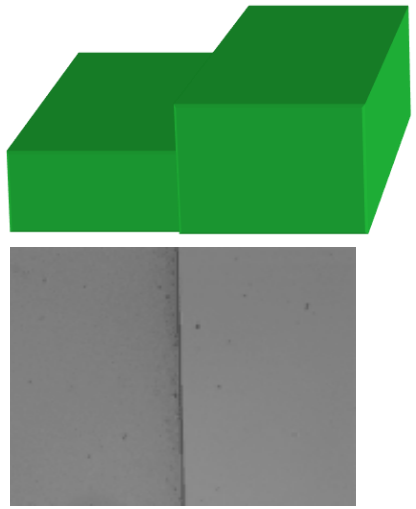
Vertical Scanning Interferometry (VSI)

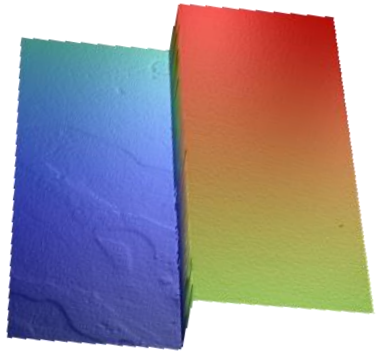


Broad Wavelength White Illumination

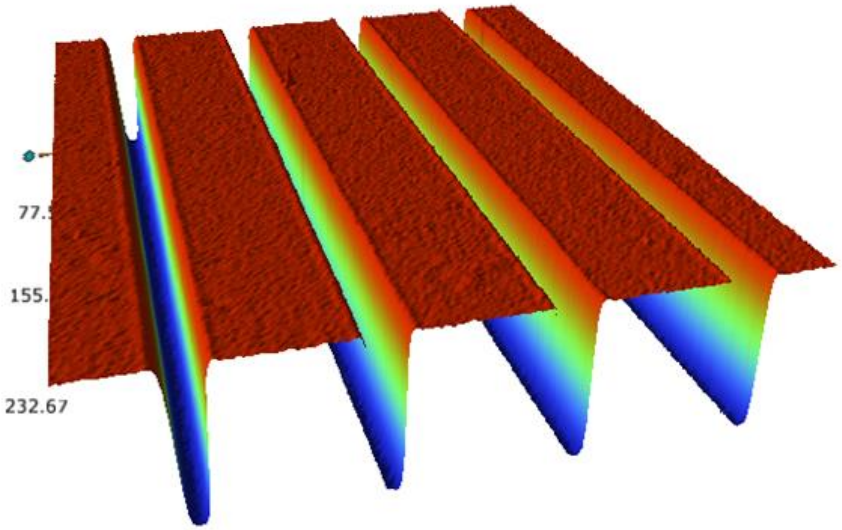
Vertical Scanning Interferometry Up to 122 µm/s

- Vertical Scanning Interferometry (VSI) is most applicable for moderately rough to very rough surfaces
- Most versatile methodology
- Large (10mm) scanning range
- 1 Nanometer Height Resolution
- +/- <.75% Step Height Accuracy
- <.1% Step Height Repeatability
- Suitable for Steep Slopes



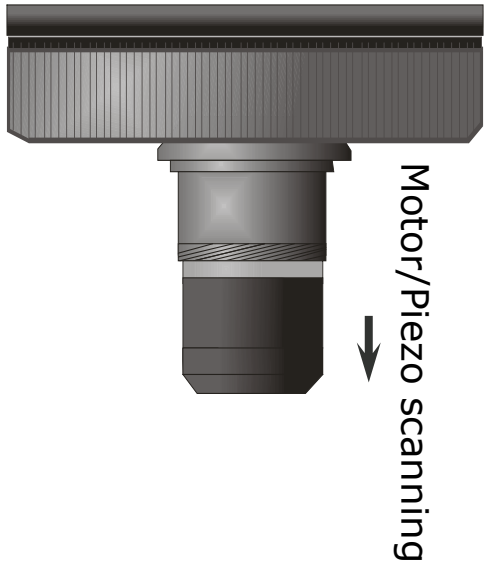


Moiré exactly tells which datapoint are in focus

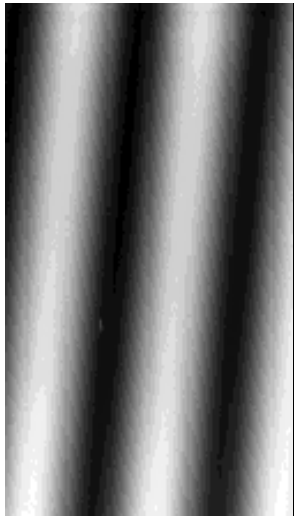


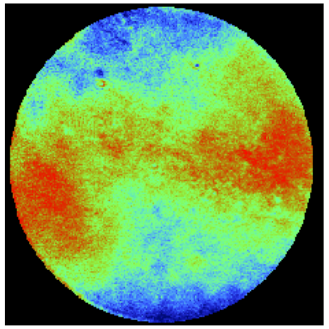
Phase Shift Interferometry (PSI)

Monochromatic illumination

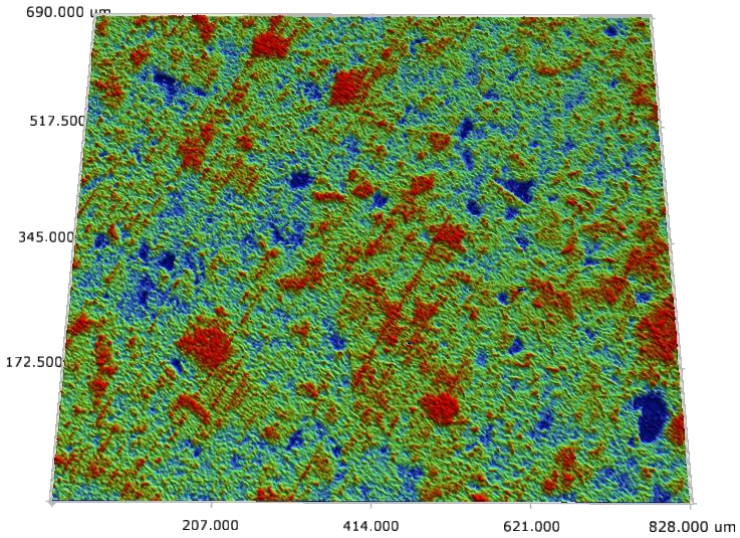


Phase Shifting Interferometry < 1 second



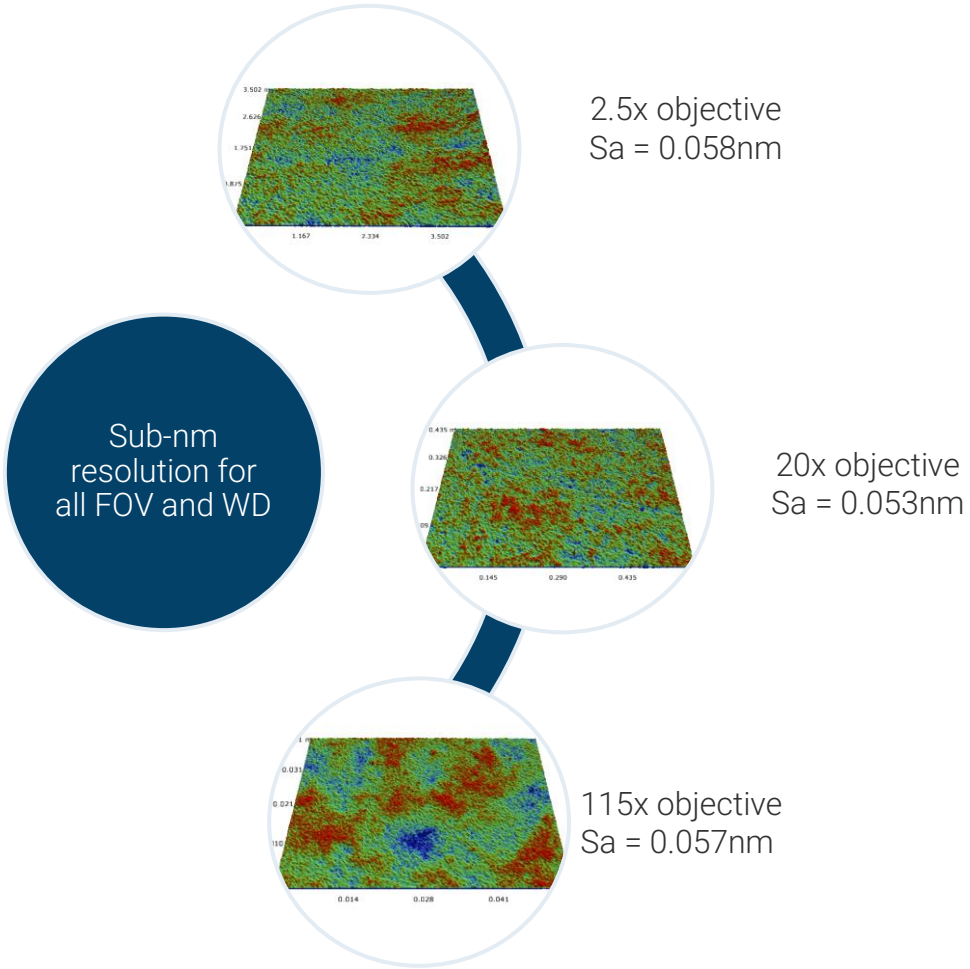


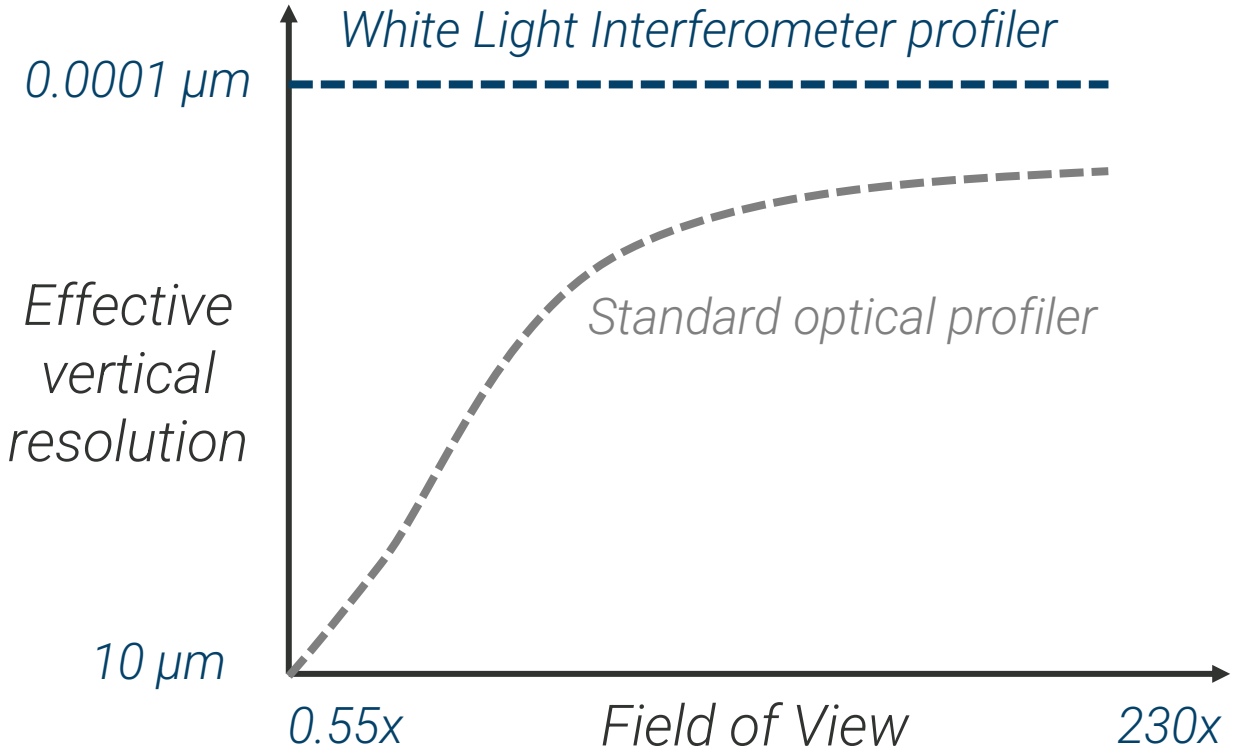
- Phase Shift Interferometry (PSI) is limited to smooth surfaces
- Ultra-High Resolution (.01nm)
- Limited Scanning Range (single micron-level)



Glass Mirror
Sa = 0.098nm

Unmatched Vertical Resolution Without Compromise



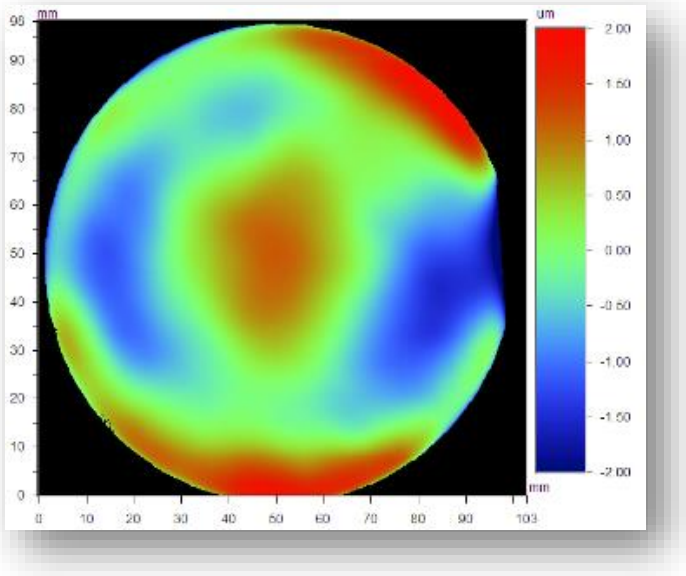


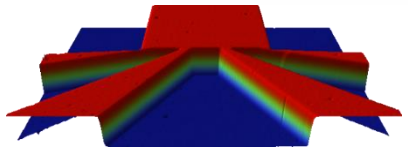
Best Vertical Metrology

White Light Interferometric Profiler
Single head – multi mode concept

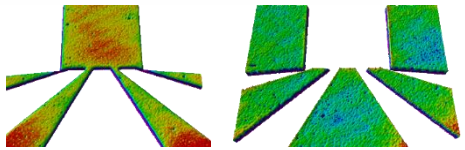
- Multi-scale: lateral

4'' sapphire wafer
Full Stitching



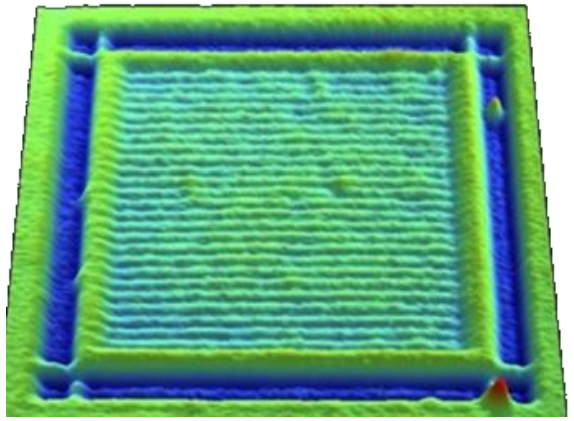


µm step



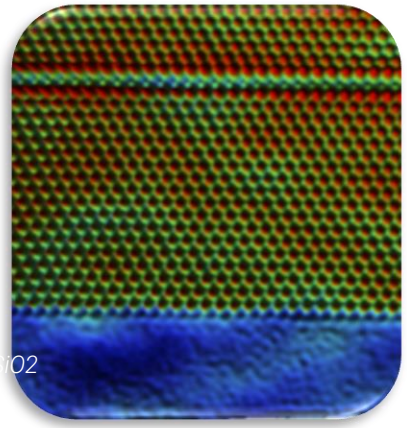
Sub-nm roughness

- Ultimate lateral resolution

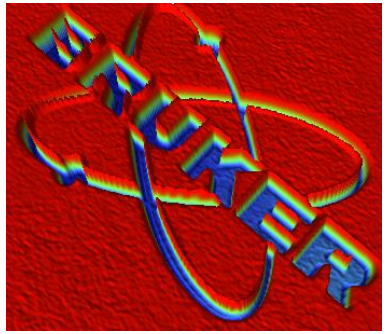


200nm spaced lines

Chromium on glass



190nm diameter spaced by 900nm



- Multi-scale: vertical
- Simultaneous Optical Inspection

3D Optical Microscopy Hardware

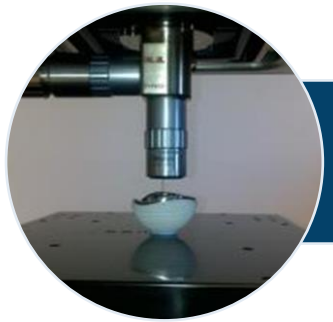
- Benchtop

- Stand alone

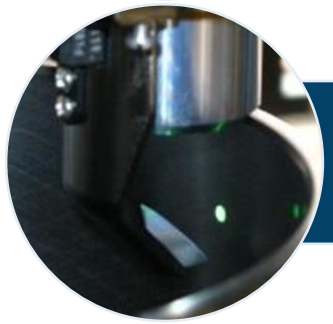
- Semiconductor Fabrication

Universal Metrology for All Surfaces

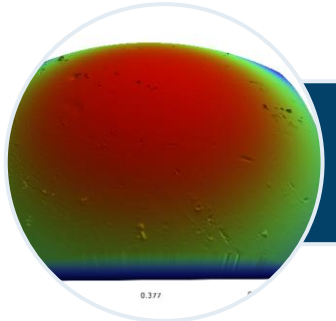
Safe operation @
high magnifications



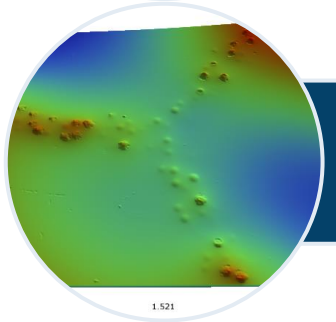
Improve access
with LWD objectives



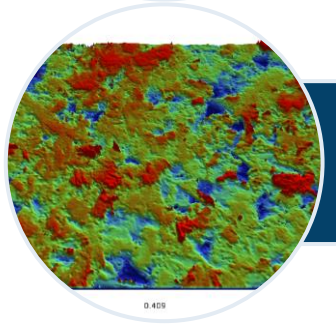
Access vertical walls



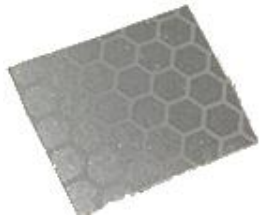
Shiny & Curved



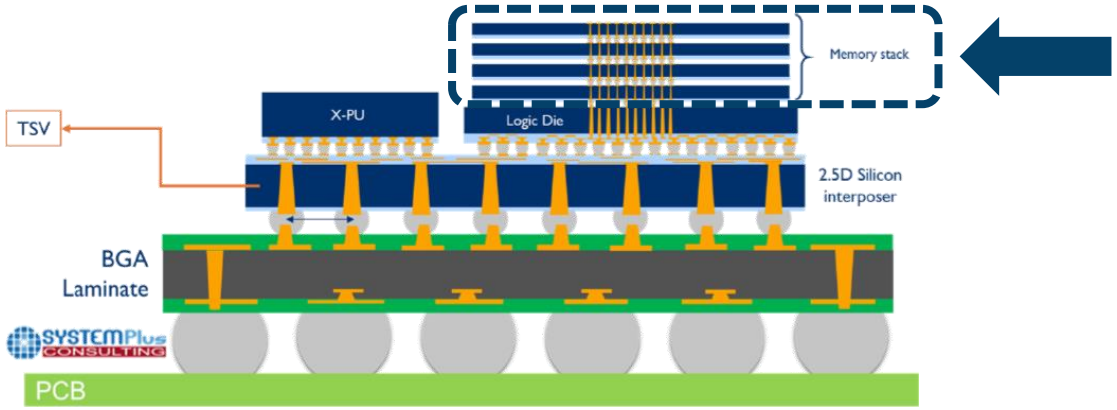
Transparent



Black color



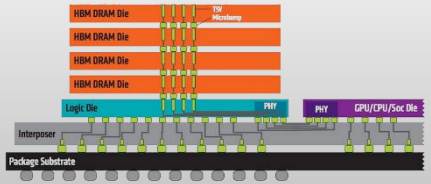
Die / Wafer stacking optimization



Die Flatness
Complex CMP process

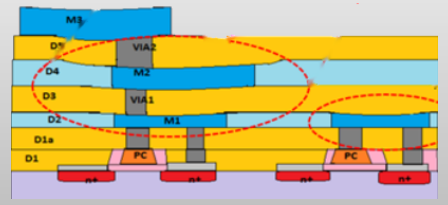
Hybrid & Wafer Bonding

3D & Advanced Packaging

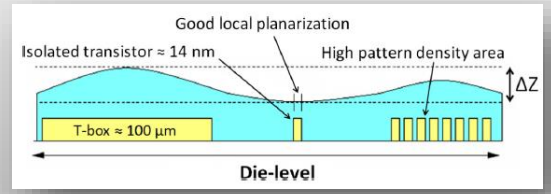


Full Die topography

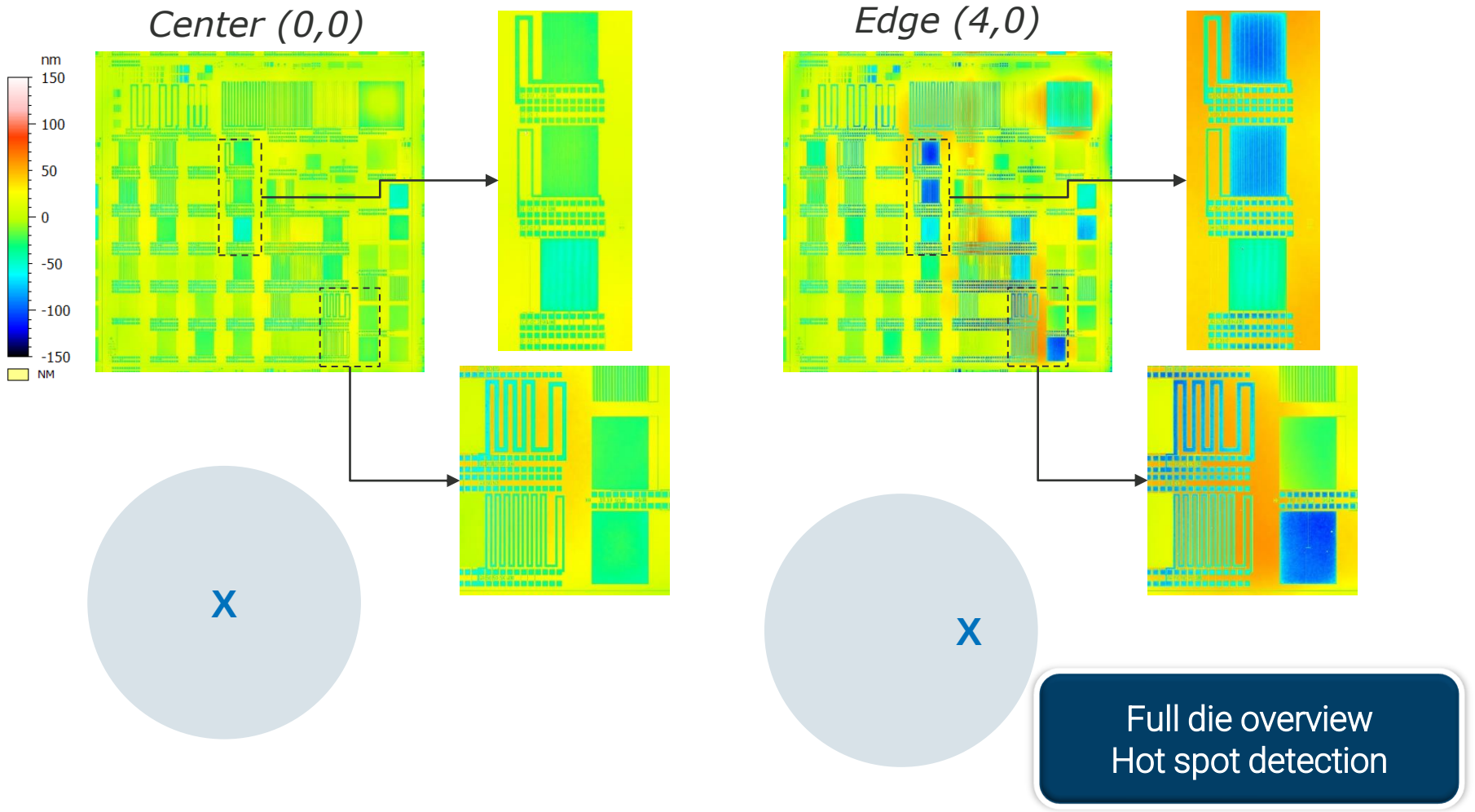
Layer stacking



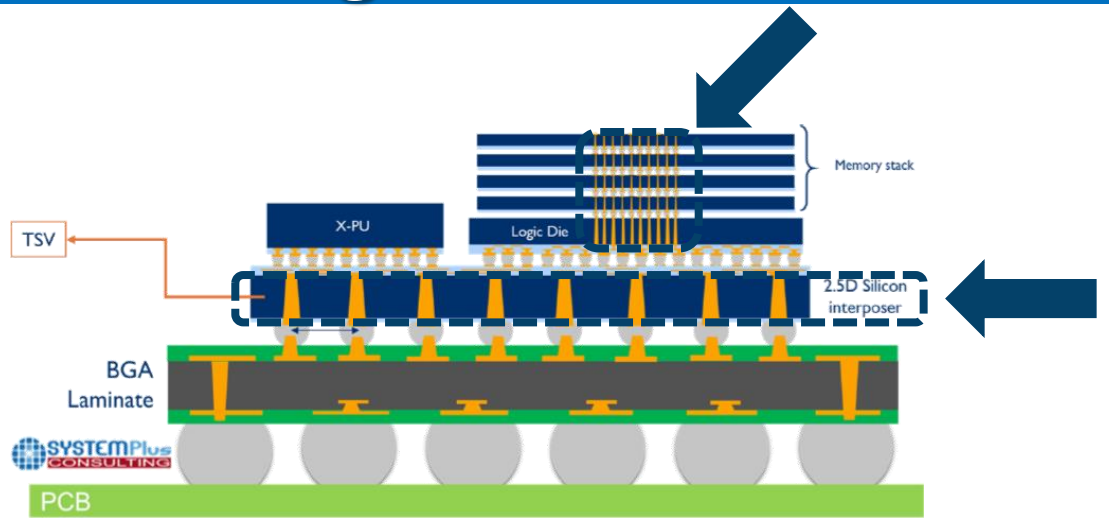
CMP optimization



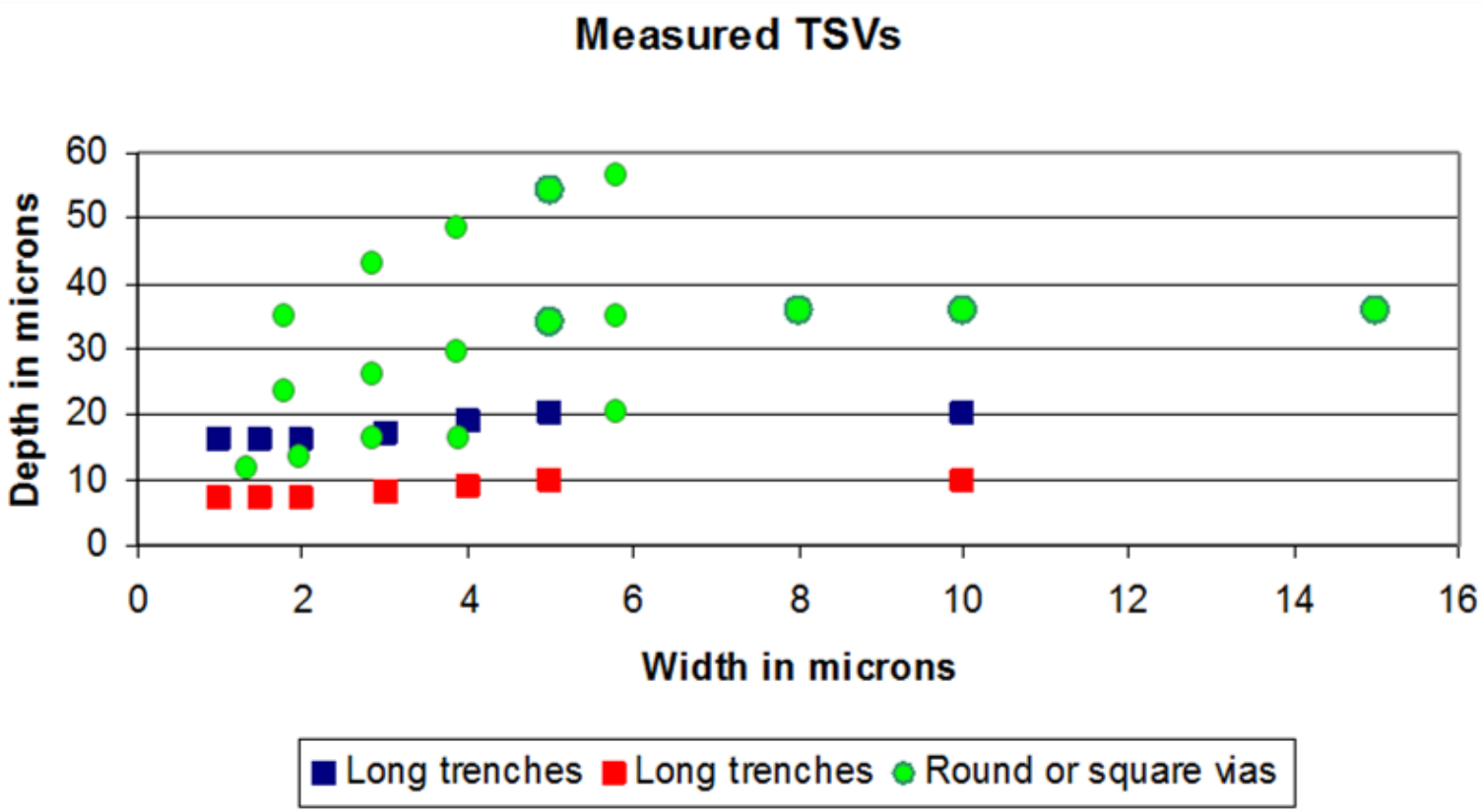
Full Die Stitching with WLI Profiler
Pattern & die position effects



Through Silicon Via



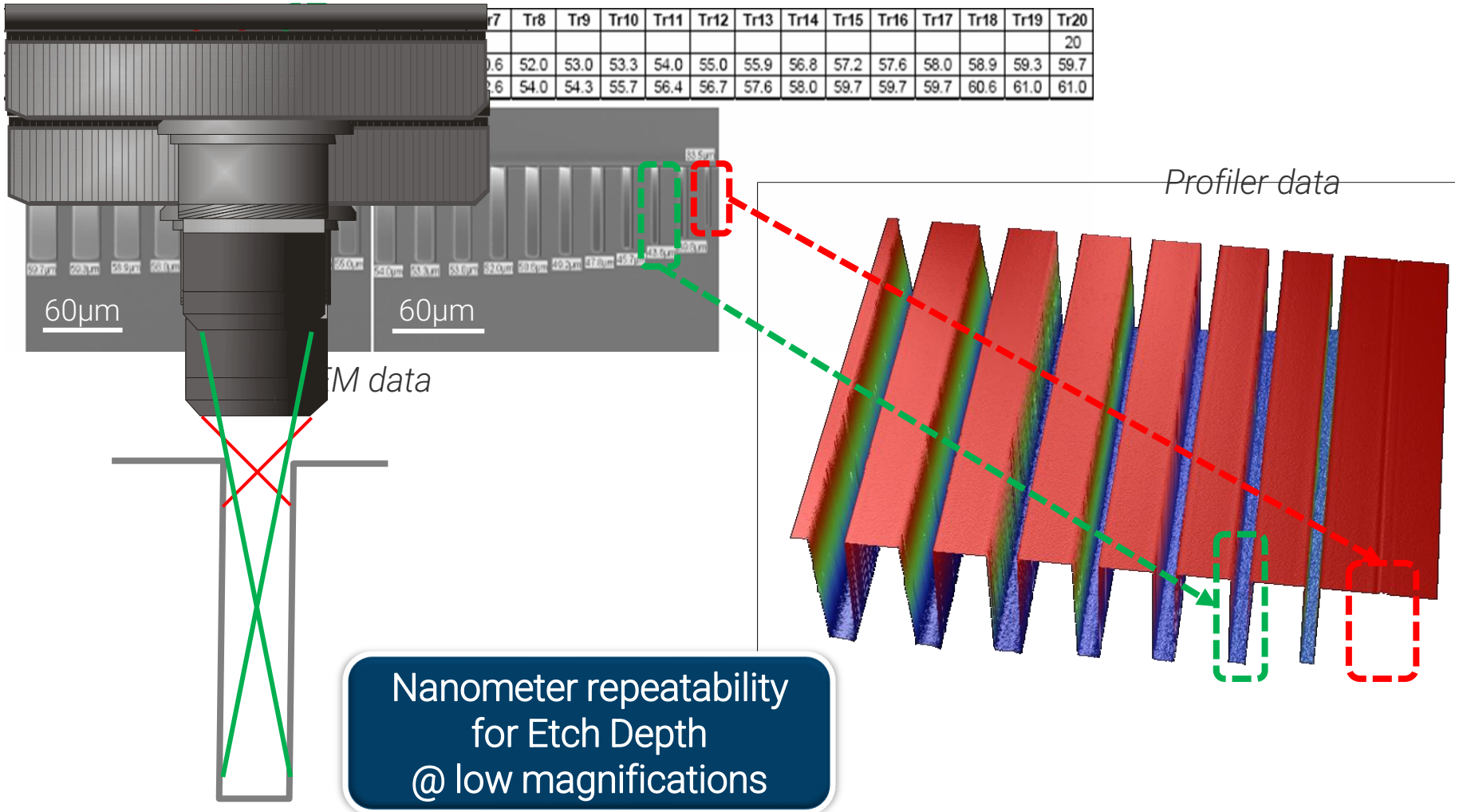
Through Silicon Via (TSV)
Measurement space



Proven wide capabilities up to 1:20

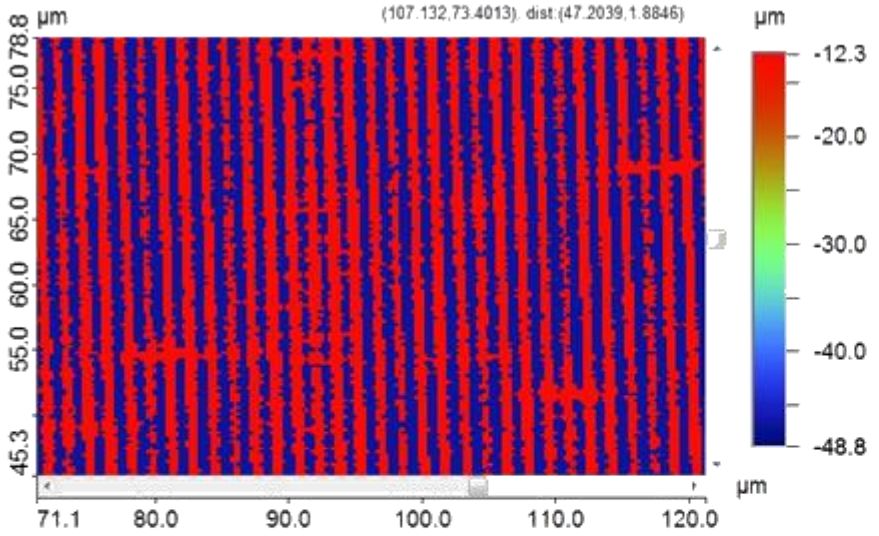
High Aspect Ratio Trench
Correlation with SEM cross-section

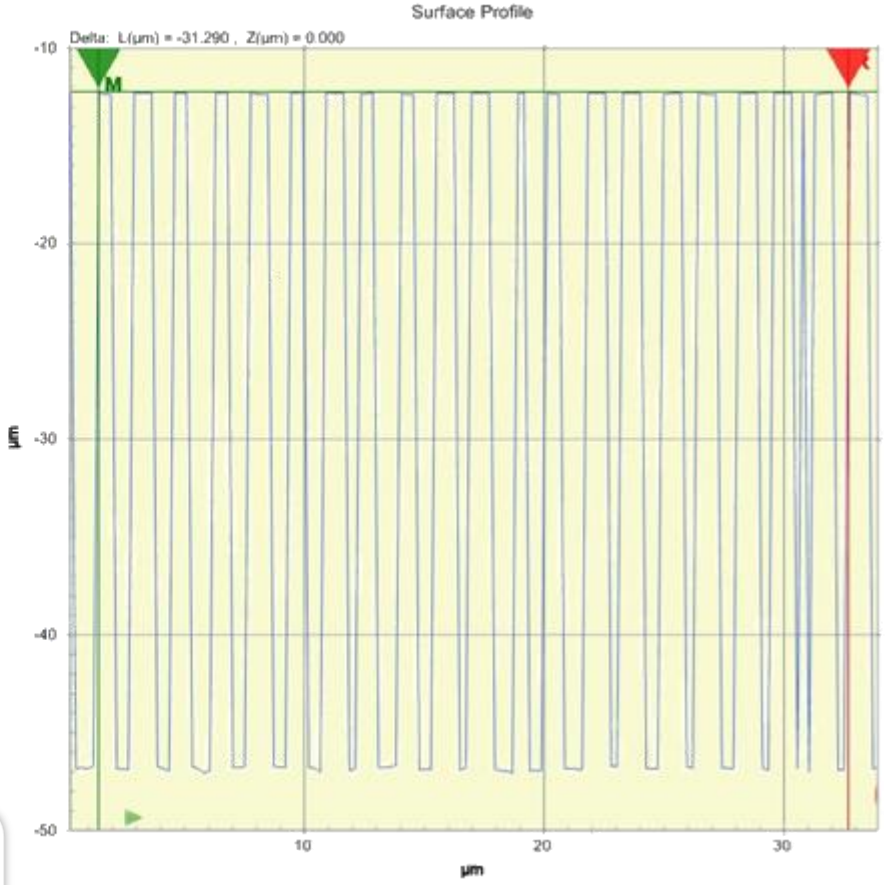
	Tr8	Tr9	Tr10	Tr11	Tr12	Tr13	Tr14	Tr15	Tr16	Tr17	Tr18	Tr19	Tr20
													20
.6	52.0	53.0	53.3	54.0	55.0	55.9	56.8	57.2	57.6	58.0	58.9	59.3	59.7
.6	54.0	54.3	55.7	56.4	56.7	57.6	58.0	59.7	59.7	59.7	60.6	61.0	61.0



Nanometer repeatability
for Etch Depth
@ low magnifications

High Aspect Ratio Trench
Extreme case

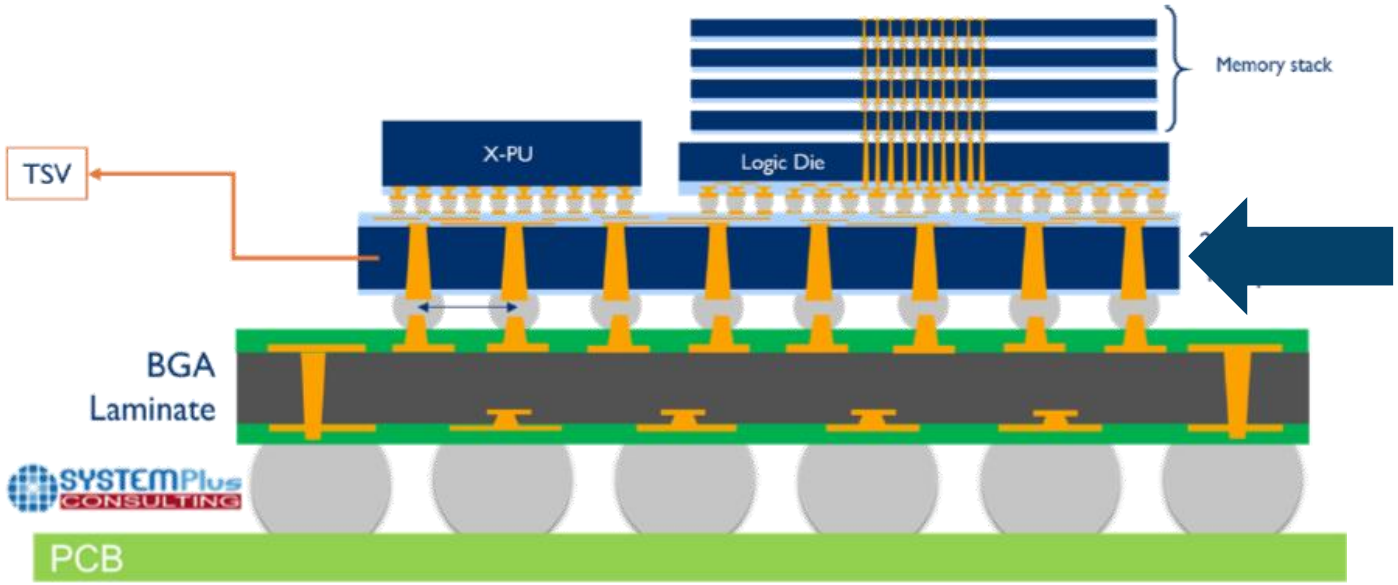




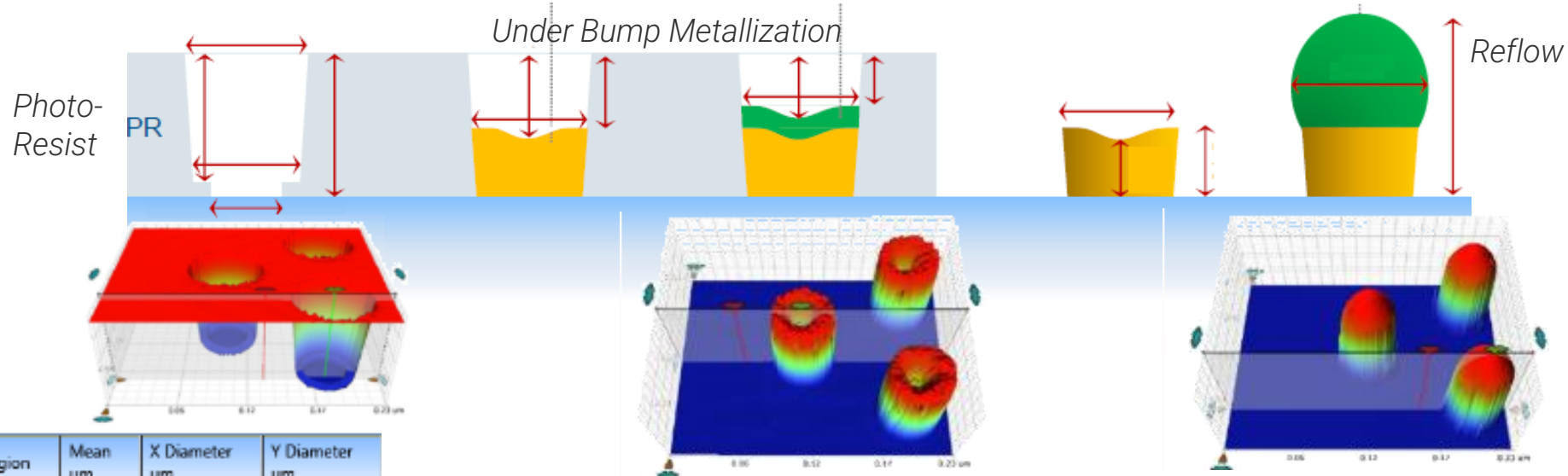
Pitch: 1.5 µm
Width: 1.5 µm
Depth: 34 µm
Aspect Ratio: 1:20

Nanometer vertical repeatability

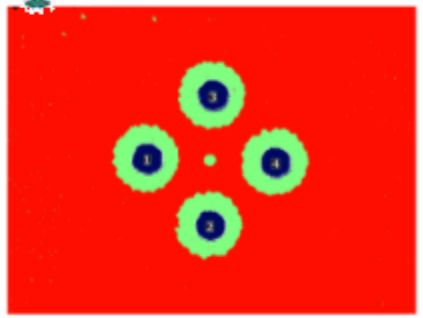
Bumps



Copper Pillar / Solder Bumps Height Width and Photo Resist Thickness



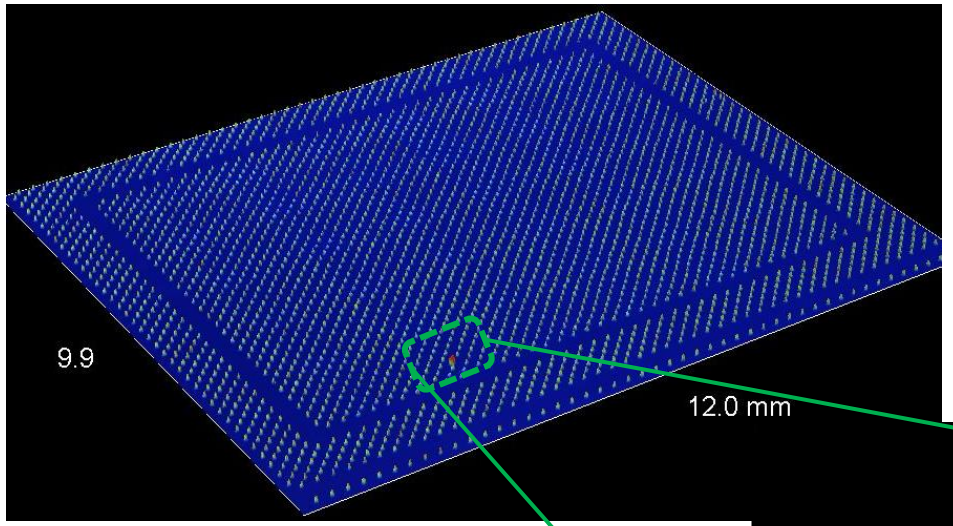
No	Region	Mean µm	X Diameter µm	Y Diameter µm
1		-60.841	401.050	414.784
2		-59.439	403.797	406.544
3		-61.694	406.544	406.544
4		-58.657	74.167	68.673
5		-60.558	406.544	403.797



No	Region	Mean µm	X Diameter mm	Y Diameter mm
1		-127.365	0.195	0.192
2		-127.831	0.187	0.187
3		-127.908	0.201	0.195
4		-128.990	0.187	0.190

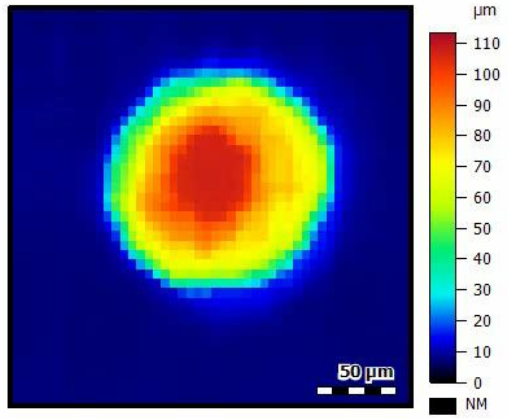
One head & Fast throughput
Nanometer repeatability

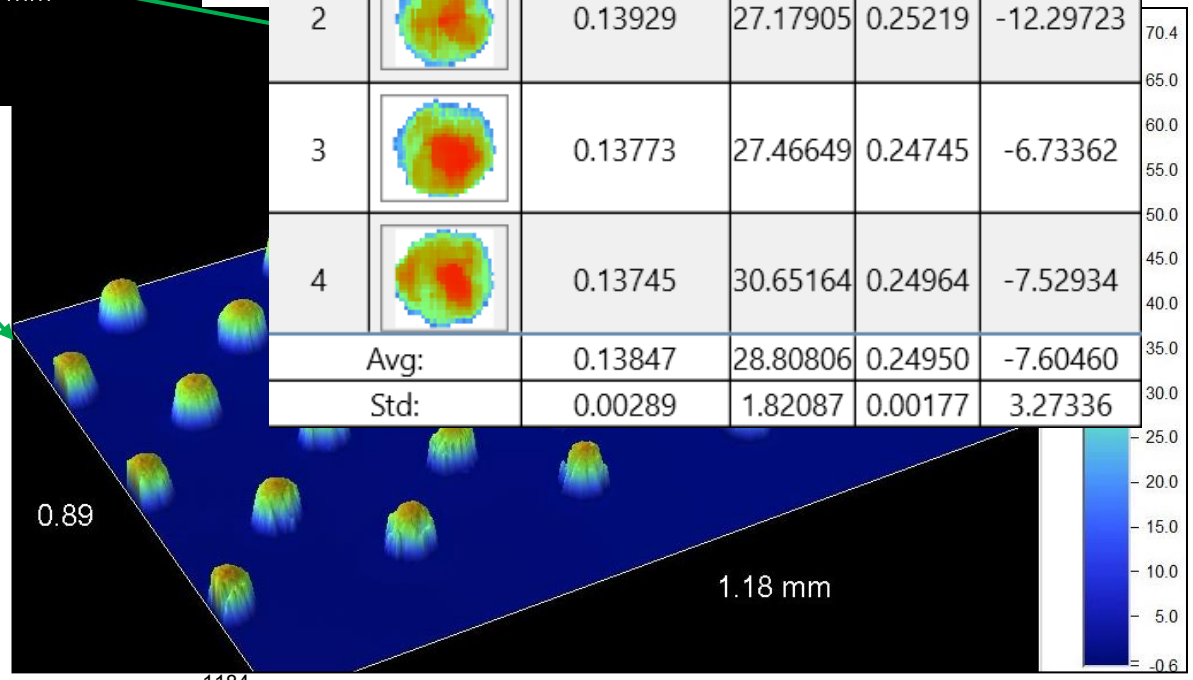
Bump array on full die
Coplanarity & Defect



Shape Accuracy
Robust metrology independent from color/reflectivity

No					ean
1					0.00000
2		0.13929	27.17905	0.25219	-12.29723
3		0.13773	27.46649	0.24745	-6.73362
4		0.13745	30.65164	0.24964	-7.52934
Avg:		0.13847	28.80806	0.24950	-7.60460
Std:		0.00289	1.82087	0.00177	3.27336

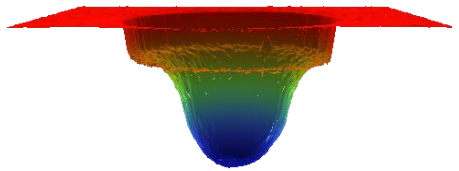




Fan-Out Packaging- Overlay Application
Production Process Control

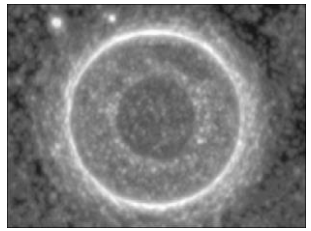
Single acquisition

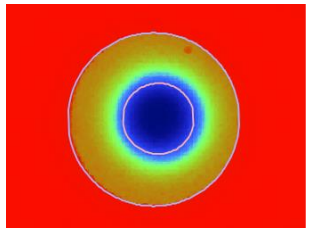
Topography



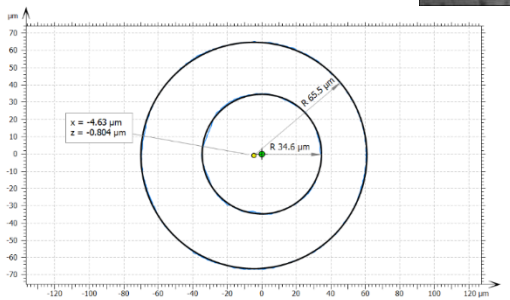
One head
<20nm Overlay reproducibility

Optical Inspection





Bottom Ra	4.817	µm
Top Ra	0.458	µm
Via Max Depth	72.294	µm
Via Mean Depth	63.332	µm
Via Min Depth	43.611	µm



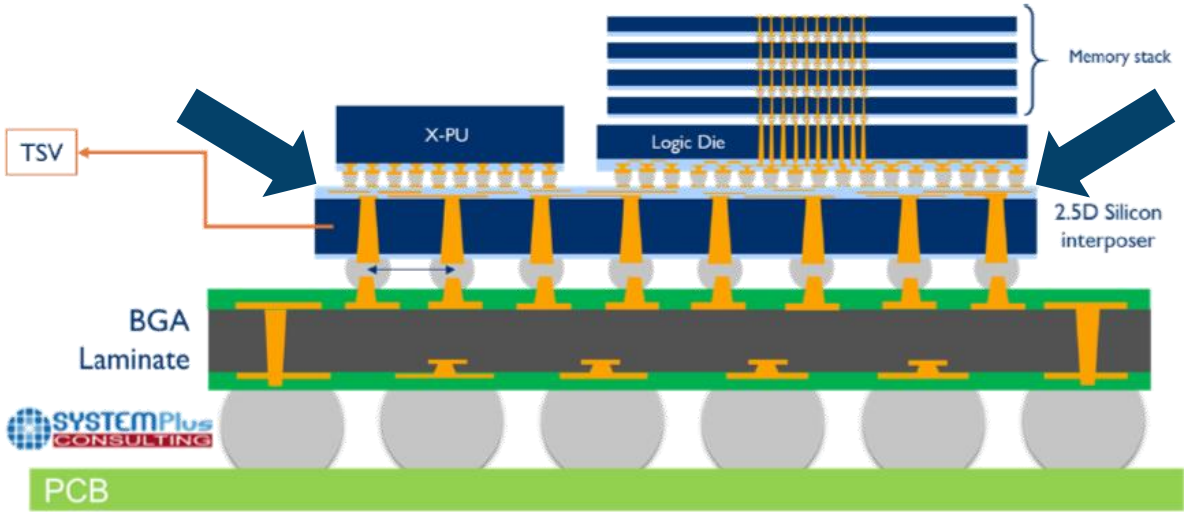
Point coordinate Overlay Offset	
x	-1.17 µm
z	0.512 µm
Dimension Inner Diameter	
Diameter (Rabs)	61.959 µm
Dimension External Diameter	
Diameter (Rabs)	147.118 µm

Same database

Database

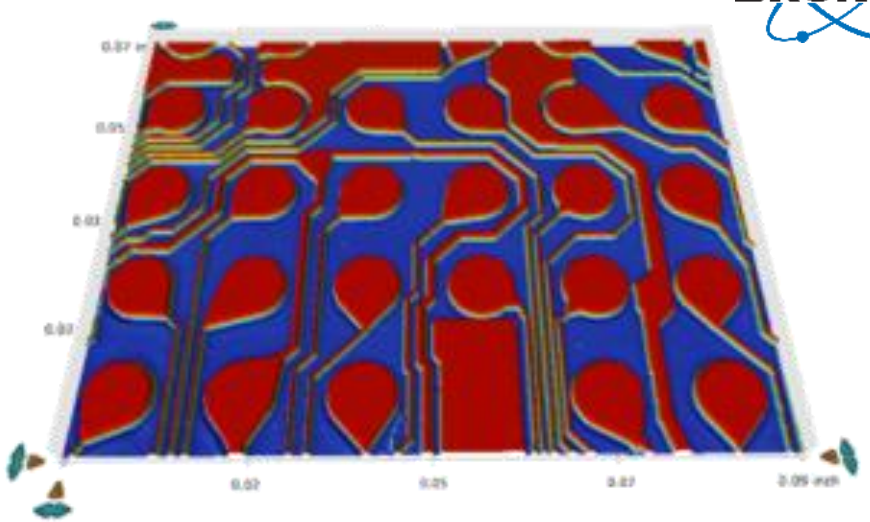
Measurement Number	Bottom Ra µm R: N/A M: N/A Always Always	Top Ra µm R: N/A M: N/A Always Always	Via Mean Depth µm R: N/A M: N/A Always Always	Overlay Offset X µm R: N/A M: N/A Always Always	Overlay Offset Y µm R: N/A M: N/A Always Always	Outer Ring Diameter µm R: N/A M: N/A Always Always	Inner Ring Diameter µm R: N/A M: N/A Always Always
1	4.817	0.458	63.332	-1.168	0.512	147.118	61.959

Redistribution Layer

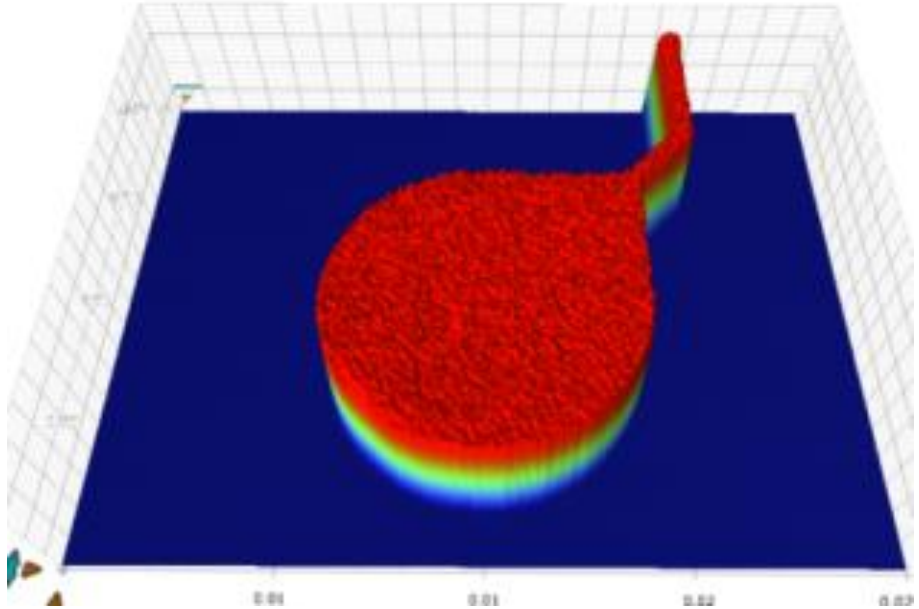


Re-distribution Layer
Fast and Repeatable Analysis

Static Repeatability	Cu thickness(um)
1	9.50
2	9.50
3	9.50
4	9.49
5	9.48
6	9.50
7	9.50
8	9.49
9	9.49
10	9.49
Average	9.49
Stdev	0.0074
Stdev%	0.08%



Tight control of Cu thickness

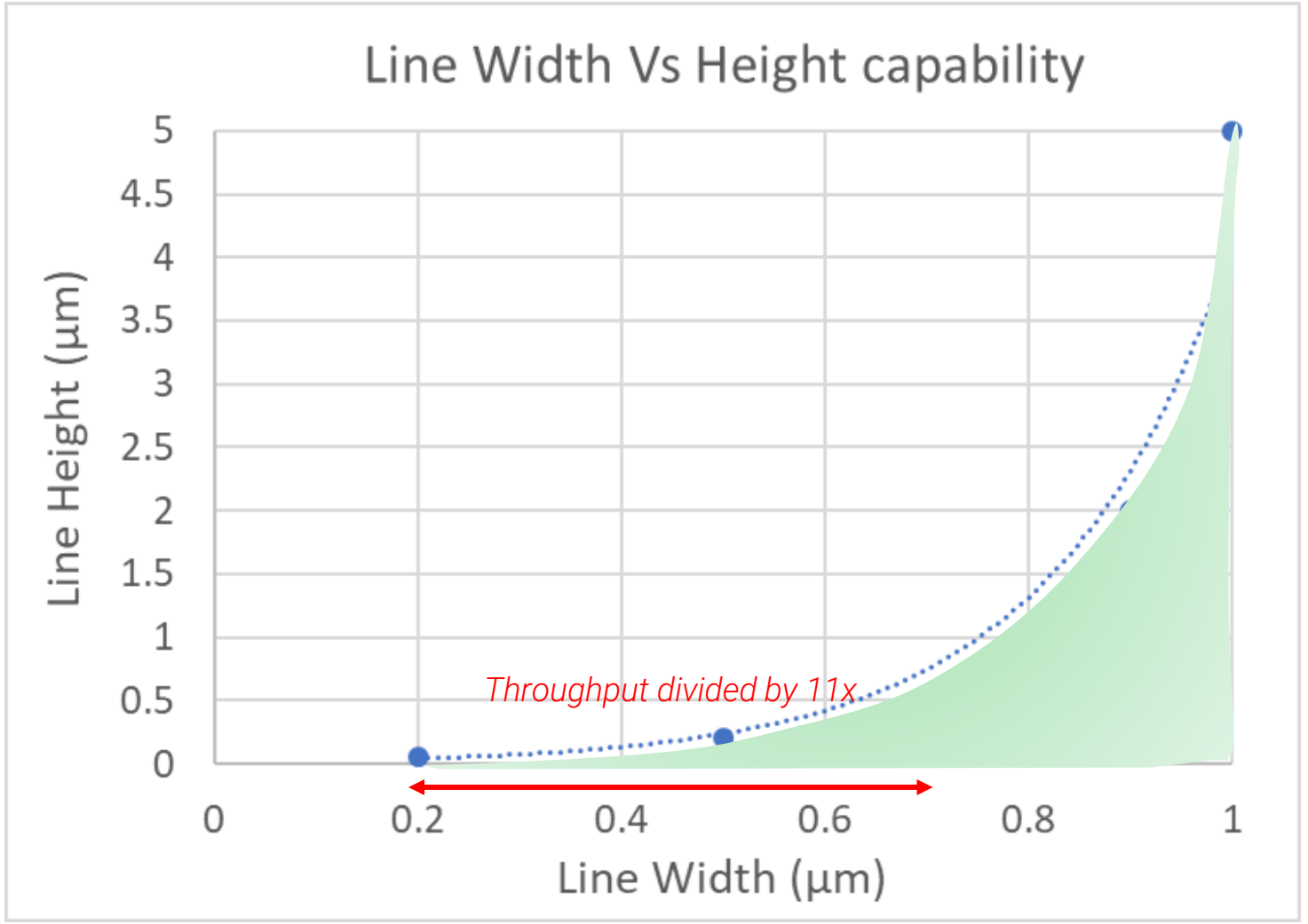


Copper Plating Thickness

Typical Performance:
<0.1% one sigma repeatability

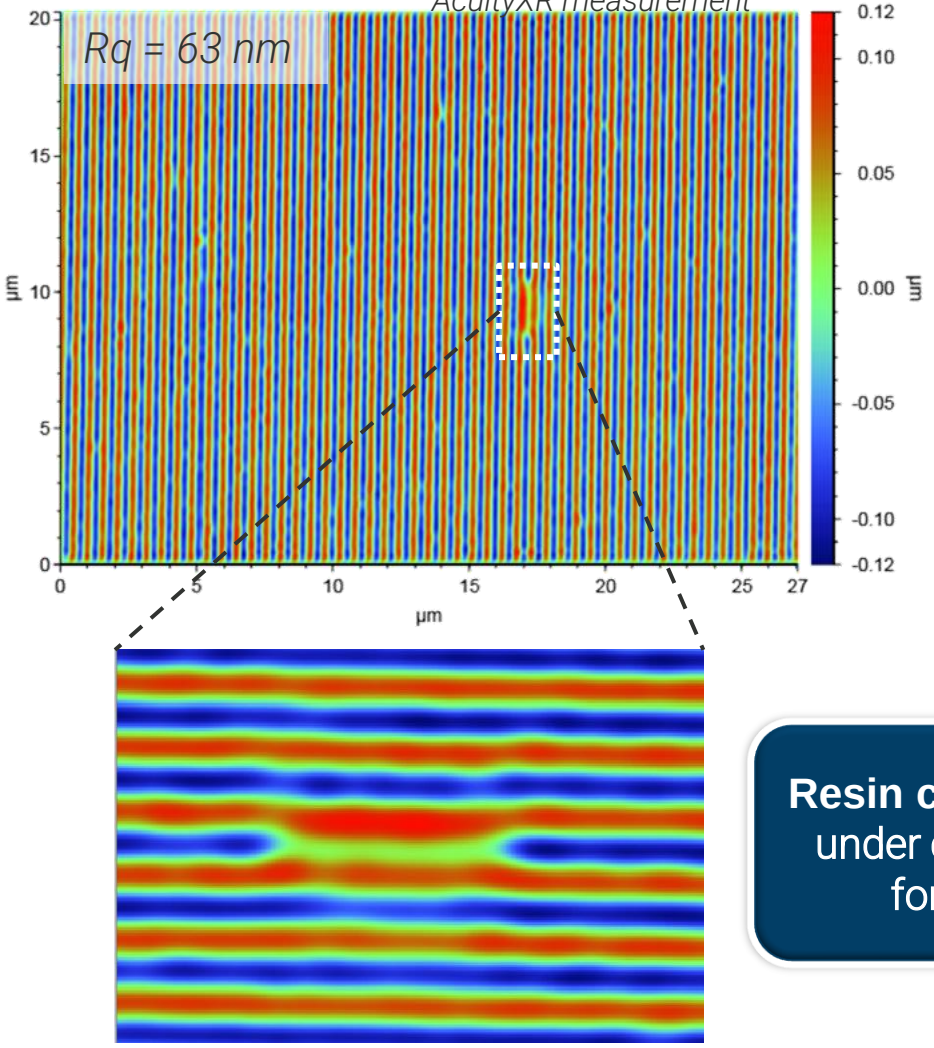
High performance metrology ensures RDL performance & quality

Line width measurement
Optical boundaries

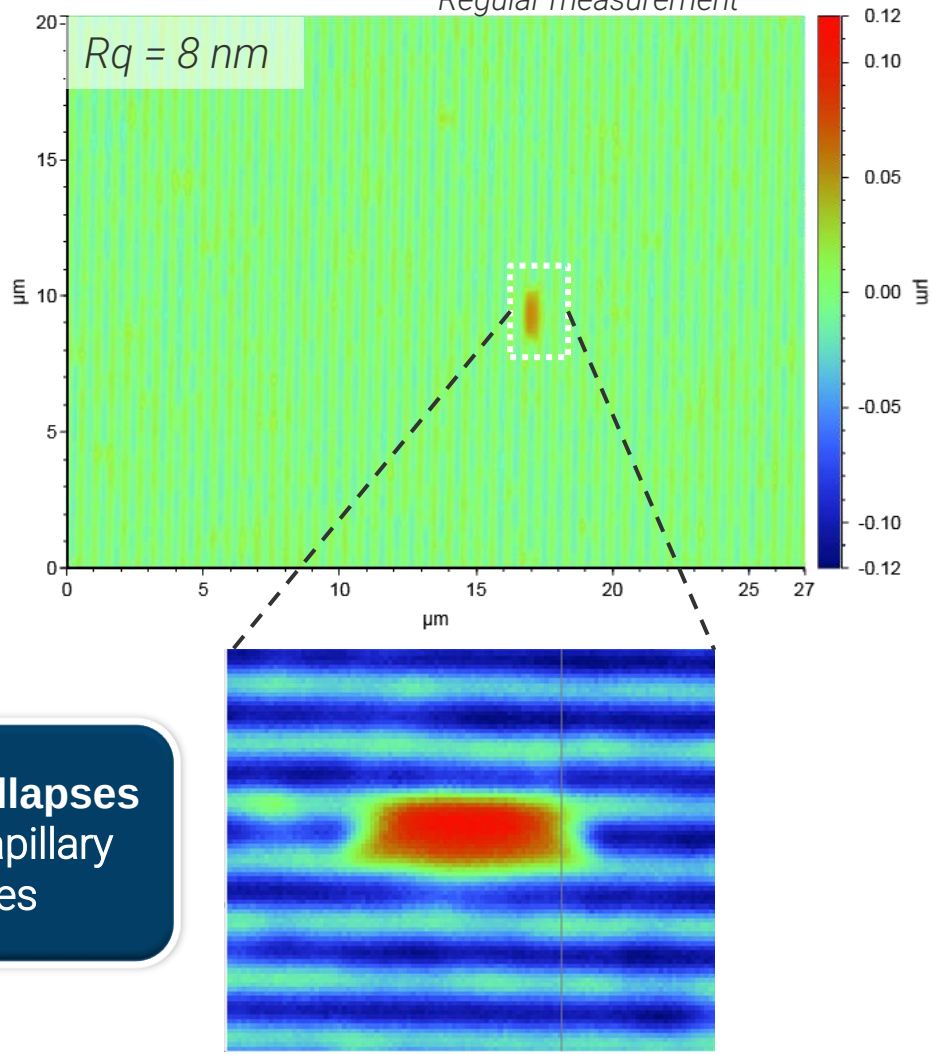


Line width measurement
True understanding of defect

AcuityXR measurement



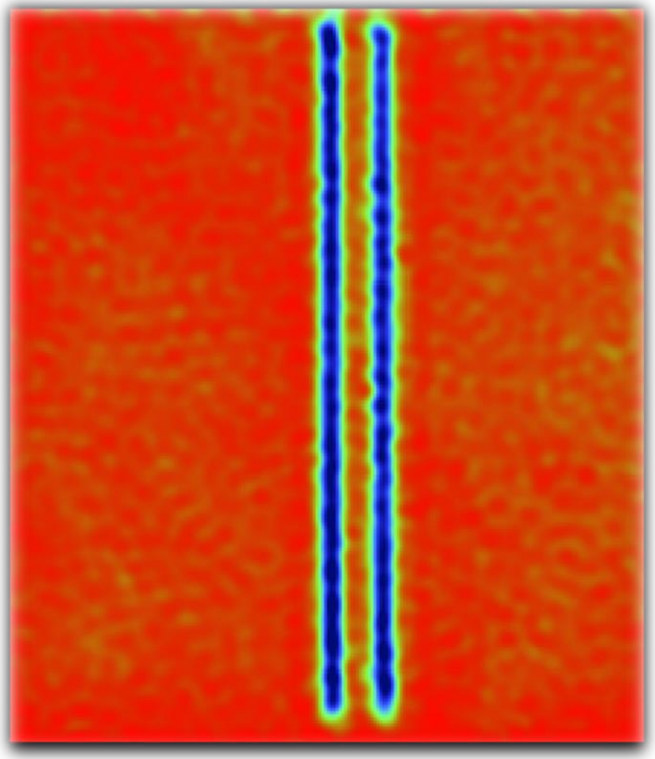
Regular measurement



Resin collapses under capillary forces

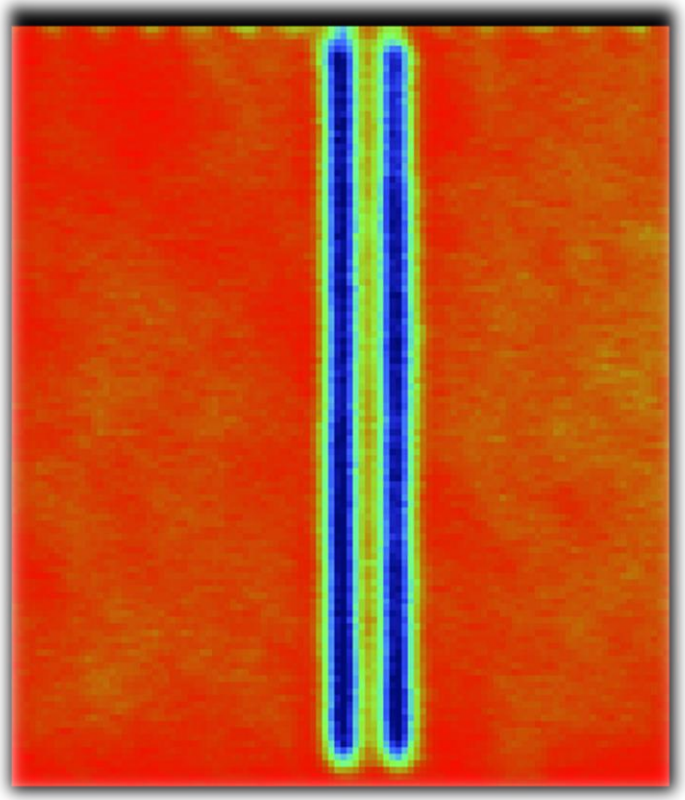
Line width measurement
Better performances in metrology

AcuityXR measurement



300nm line space

Regular measurement



11µm x 10µm
Z scale: 12nm

Parameters	Standard	AcuityXR	Improvment
Line Width Std Dev (nm)	35.16	5.27	6.7x

Summary

Wafer to Wafer bonding

Heterogeneous integration

Die Flatness

- Unique sub-nm repeatability
- Sub-micron lateral resolution
- Hot spot detection

Through Silicon Via

- Better lateral resolution than IR
- Better vertical reproducibility

White Light Interferometer Profiler

Bump

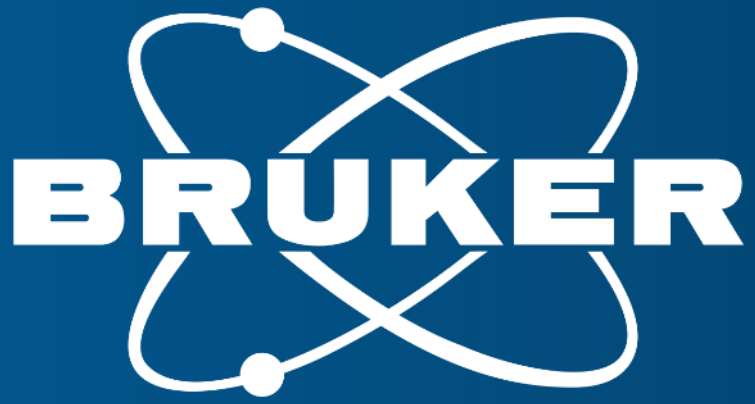
- Large field of view while retaining nanometer vertical resolution
- Sub-micron lateral resolution
- Defect map

Critical Dimensions

- <20 nm repeatability
- Up to 100nm lateral resolution
- Width, Overlay, diameter
- Throughput gain via single measurement for 2D & 3D

Interconnect

Stacking



Innovation with Integrity