Advances in Vertical Wire Bonding Enable Low-Cost Shielding and Wafer Level Interconnect Solutions

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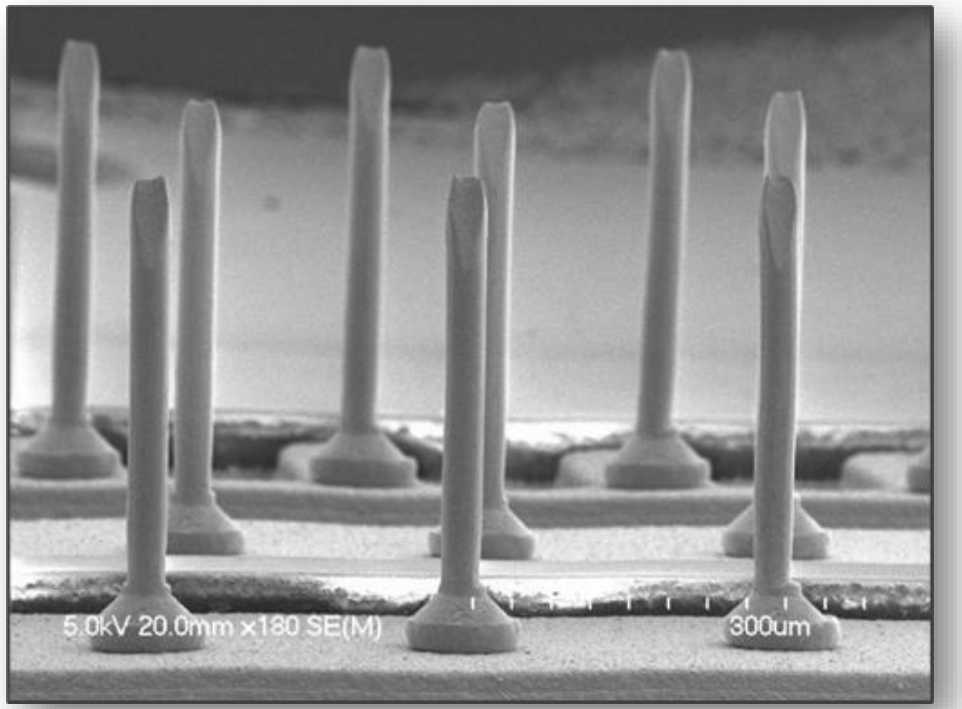
Mar 20, 2024

Kulicke & Soffa®

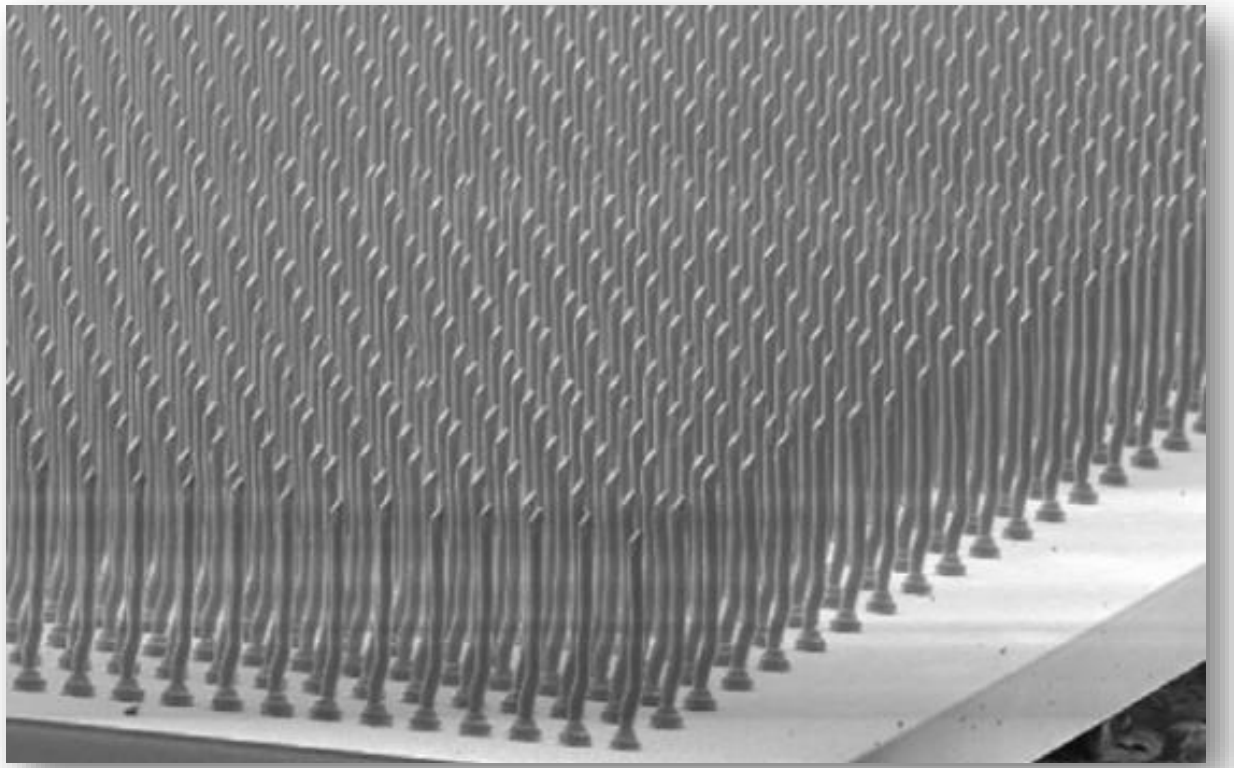
Vertical Wire Introduction

- Vertical Wires are formed using a unique process on Ball Bonder equipment for both substrate or wafer level packages
- Vertical Wires offer a lower cost package alternative to TMI, TSV, or Cu Pillar interconnect

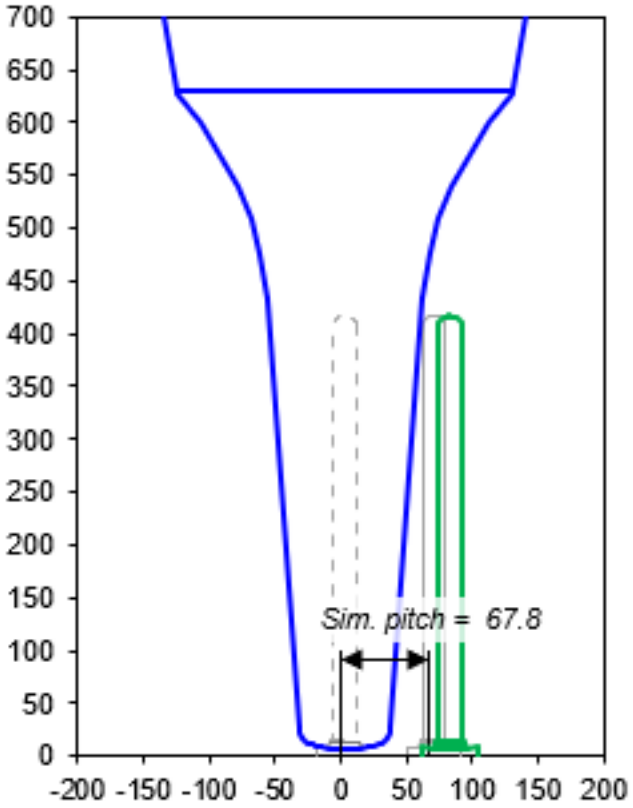


Vertical Wire Capability Range

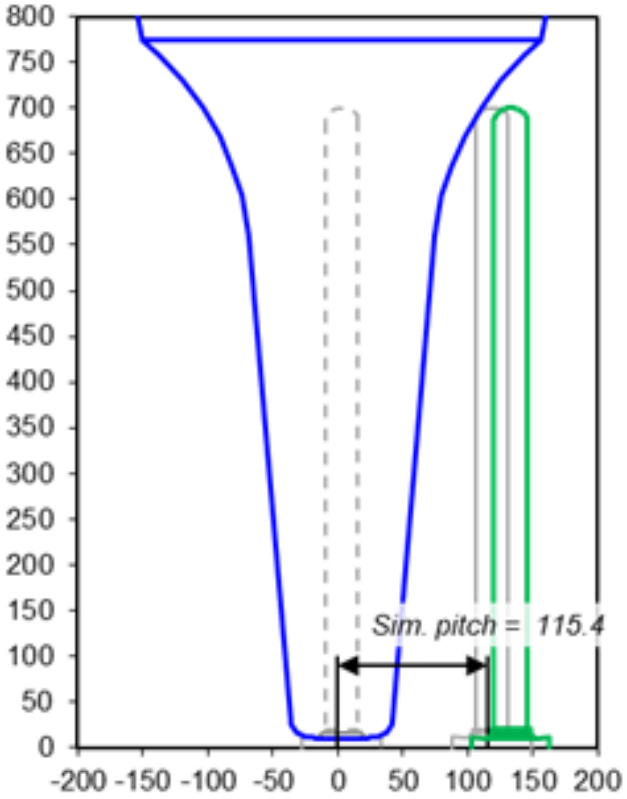
- Wire Types: Cu, PdCu, Ag, Au
- Wire Diameter: 18µm ~ 50µm
- Wire Height: 100µm ~ 1300µm
- Wire Height Repeatability: ± 10µm
- XY Repeatability (Wire Tip): ± 10µm
- Min Wire Pitch*: 50um



Enabling Finer Pitch and Taller Wires



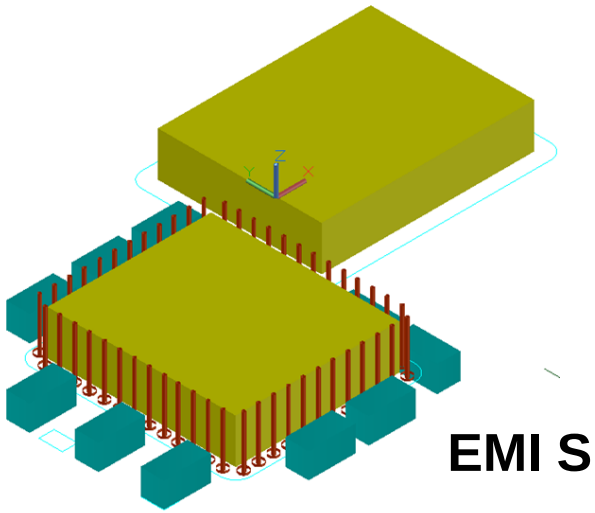
- Bonding Tool (capillary) design becomes critical when taller wire heights and/or smaller wire pitch is desired
- Greater pitch allows for taller wires and vice-versa



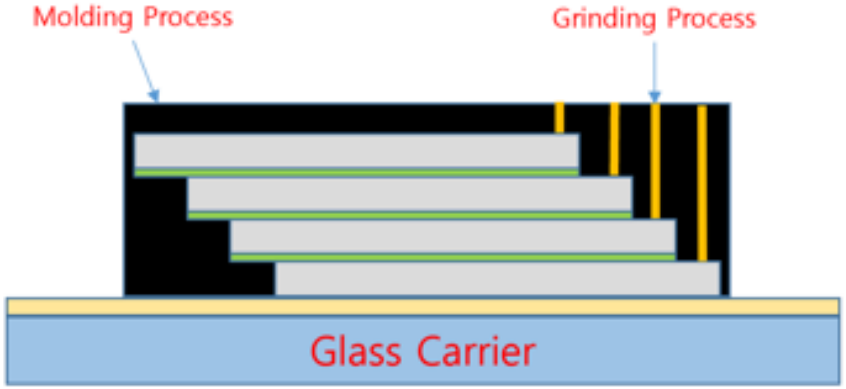
Vertical Wire Applications

- Although initially developed for interconnection applications, Vertical Wire was introduced in HVM for EMI shielding in SiP and RF packages

- Multiple evaluations currently in progress to qualify using Vertical Wire as a through mold interconnect or potentially replace Cu Pillar

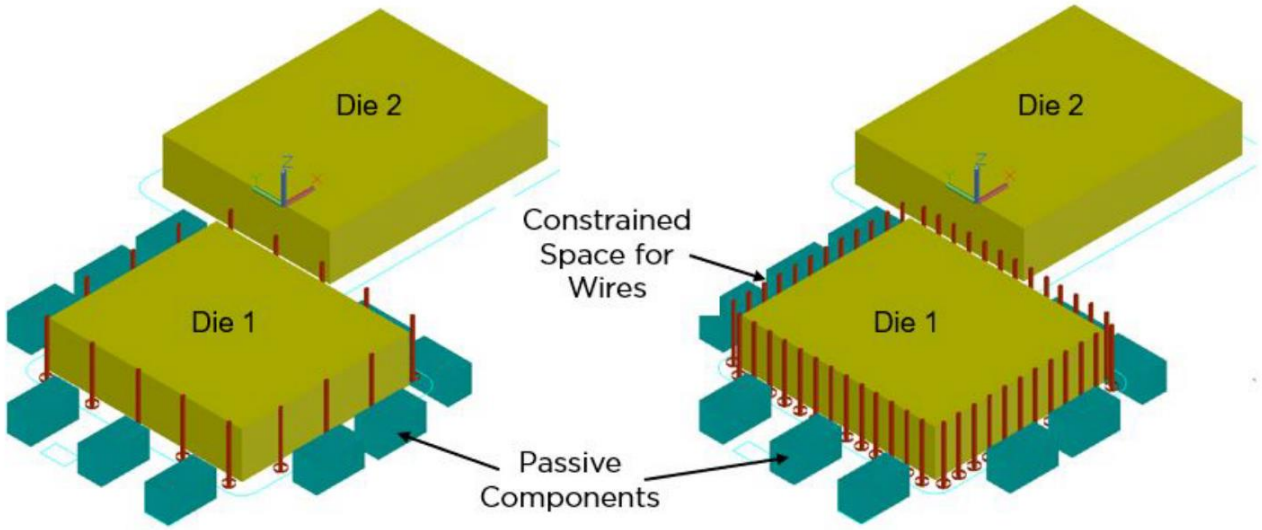


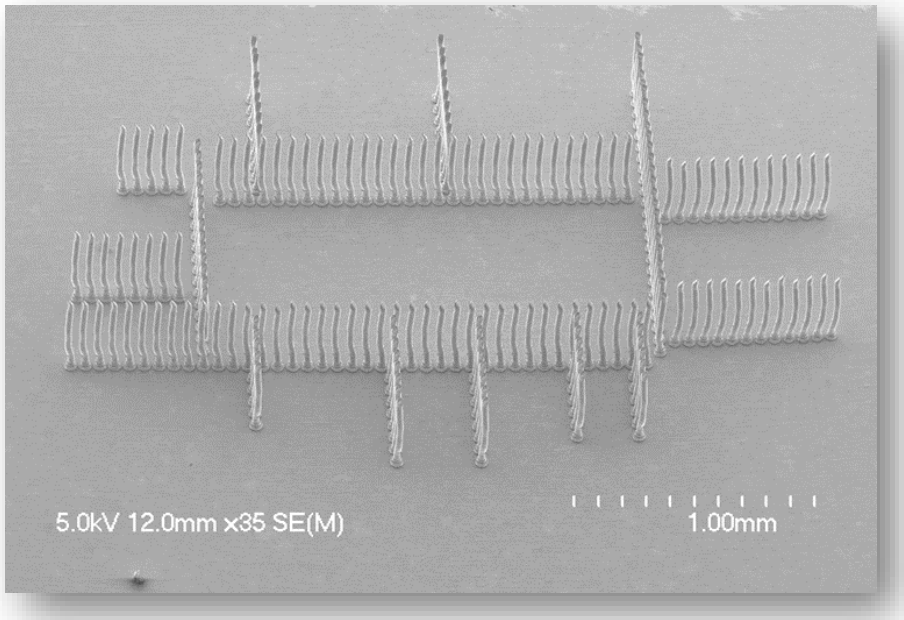
EMI Shielding



Through Mold Interconnect

Vertical Wires Used in Shielding

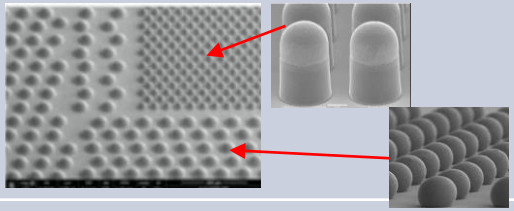
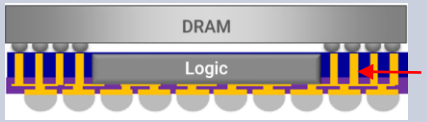
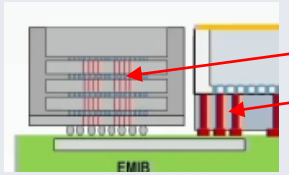




Compartmental Shielding with Vertical Wires

- Shrinking package sizes move components closer together, driving the need to prevent electromagnetic interference (EMI) for RF packages
- Vertical Wires are typically connected to an outer conformal shield layer

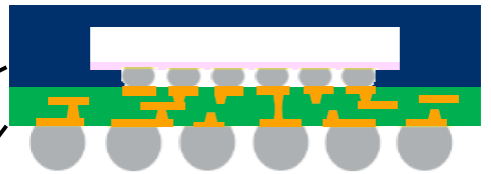
Vertical Wire as Potential Alternative

Interconnection	Applications	Comments
uBump (Cu Pillar + solder) ✖		Requires smaller bump pitch (< 30um) and improved accuracy
UBM + C4 ✖		Batch process, relatively low cost, high throughput
InFO Via ☺	 InFO Via	Integrated to FEOL process, est. 17 process steps. Vertical Wire could significantly simplify process flow
TSV ☺	 TSV HBM TSV Si Interposer	Vertical Loop is a low-cost alternative to TSV for stack die application Disadvantage : potentially larger footprint
Cu Pillar ☺	PoP interconnection InFO PoP	Vertical Loop is a low-cost alternative to Cu Pillar Requires wide range of diameter requirements (20um to >200um)

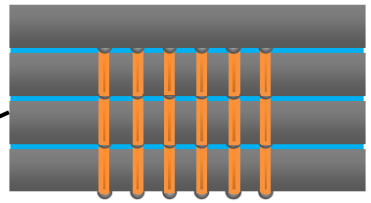
Memory Package Comparison

Package Type	Process	End Applications
DDR5, DDR6	Single die Mostly Flip Chip Some remain WB for DDR5	Server, PC/consumer, Automotive (ADAS)
G-DDR6, G-DDR7	Single die Flip Chip	Graphics, AI inference, Automotive (ADAS), Network
HBM2, HBM3	Multi die 3D Fan-In WLP with TSV	HPC, AI Training, High speed network
LPDDR4 LPDDR5	Wire bond	Mobile, AI edge inference, Automotive (ADAS)
NAND	Multi die Wire Bond	SSDs for PC Data center applications

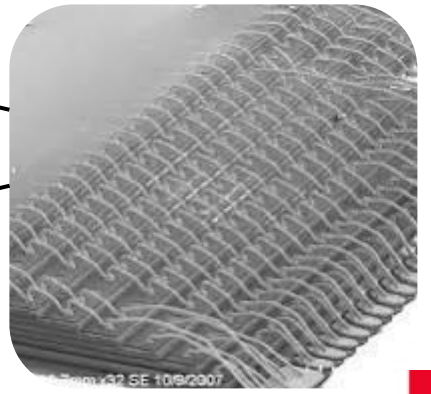
Flip Chip



TSV



Wire Bond

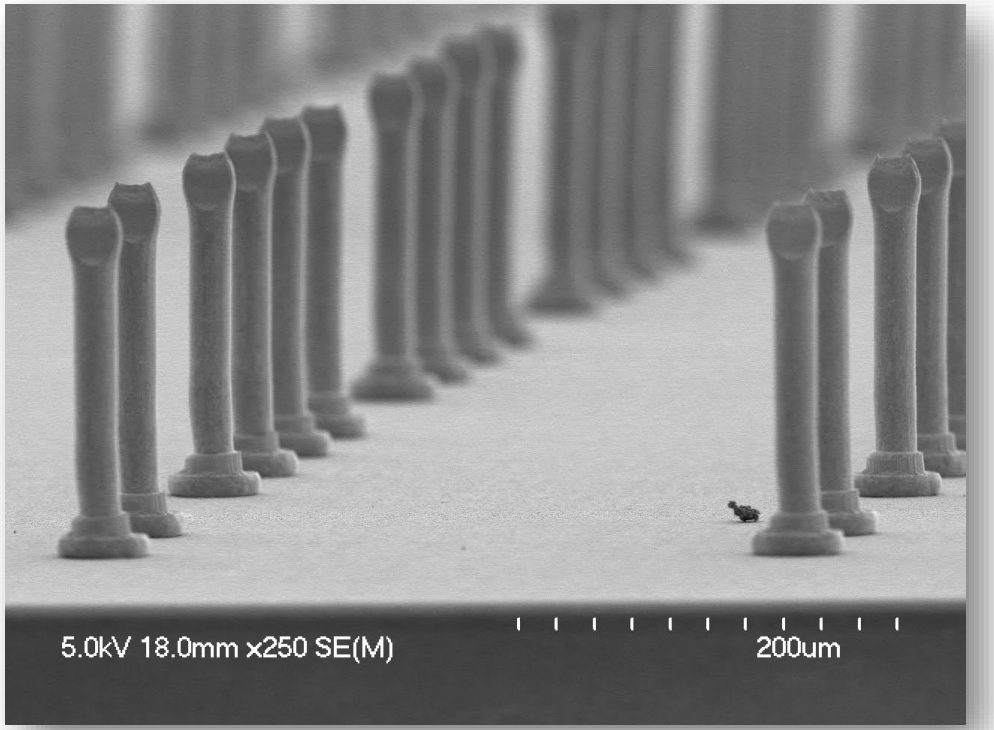


Wafer Level Wire Bonder Equipment

- Large Area Ball Bonder capable of handling 150mm, 200mm, 300mm wafers
- Integrates with Auto Wafer Handler and EFEM automation solutions

Conclusions

- Vertical Wire Bonding is fully qualified and already running in HVM for shielding applications for more than 5 years
- New concepts are emerging for using Vertical Wire as interconnect, primarily for cost reduction or package form factor
- R&D continues in equipment, materials, and process capability to enable finer wire pitch, taller wires and larger wire diameter



Questions?

Thank You!

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