From Technologies to Market

International Microelectronics Assembly and Packaging Society

Bringing together the entire microelectronics supply chain™

Advanced Packaging leading electronics industry transition into next decade

IMAPS DPC 2020

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YOLE Développement

PRESENTATION OUTLINE

- Emerging Markets & Trends
- Major shifts in Advanced packaging over last 5 years: Historical Perspective
- Leading Advanced Packaging form factors
- Supply Chain landscape / Advanced Packaging supplier Eco-system
- Emerging trends in Advanced packaging & Market Drivers for next 5 years
  - Fan-out packaging as an enabler in electronics industry transition and its role in shaping semiconductor supply chain

vt1 DIGITAL SOCIETY: NEW TRENDS & MARKET DRIVERS: EVER INCREASING INTERCONNECTEDNESS

→ *On the road to augmented intelligence*

Disruptive Technology

Motion sensing

Olfactometry

Imaging

Audio

TRENDS

CLOUD EDGE SPECIALIZATION

PC	Mobile	Smart	Robotics	Human Augmentation
1990	1995	2000	2006	2010	2014	2017	2020	2030	2040
	3D graphics cards	Deep neural network	Deep neural network with GPU	Siri	Alexa	First SoC with NPU	HW for audio AI		

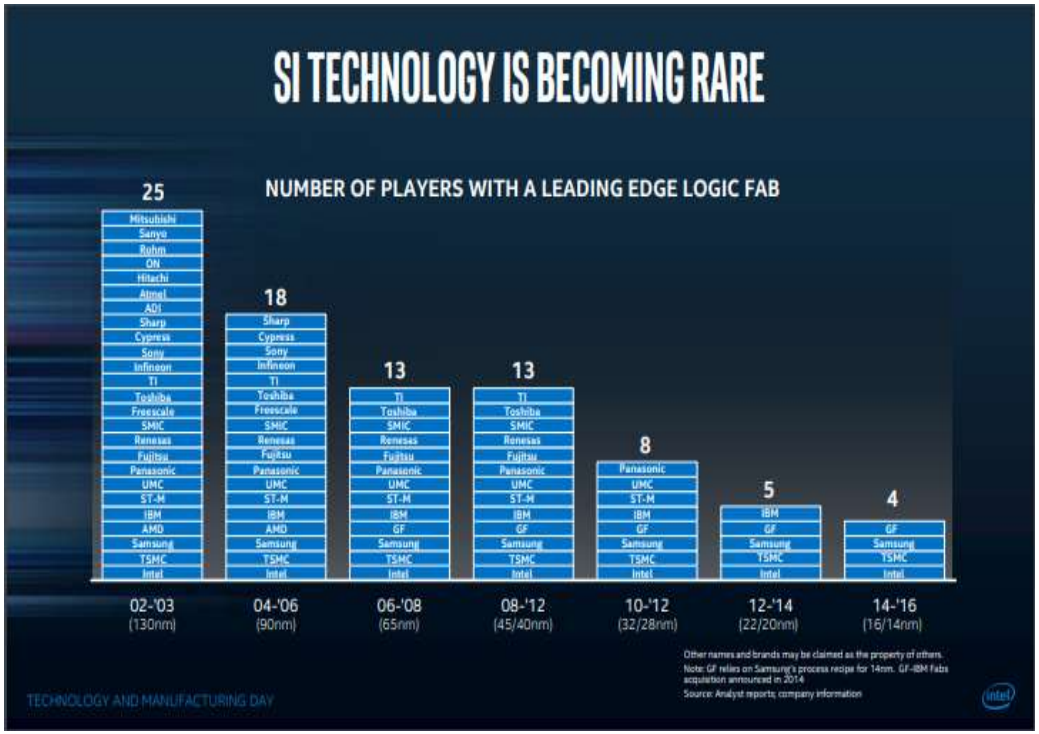
Slide 3

vt1 vaibhav trivedi, 3/4/2020

LOOKING BACK A DECADE AGO….TRANSISTOR SCALING & IC PACKAGING

Moore's law slowing down

Only 4 players with 14/12nm Fab (2017)



7nm Fab

Only 2-3 players still in the 7nm and below node race

tsmc

intel

SAMSUNG

Delay in Intel's 10nm node, so obviously they are late regarding TSMC & Samsung

Moore's law pace is slowing down, if not already dead as mentioned by Forbes & Nvidia. It's reaching some limitations as developing advanced technology nodes is doable technically but not anymore cost efficient

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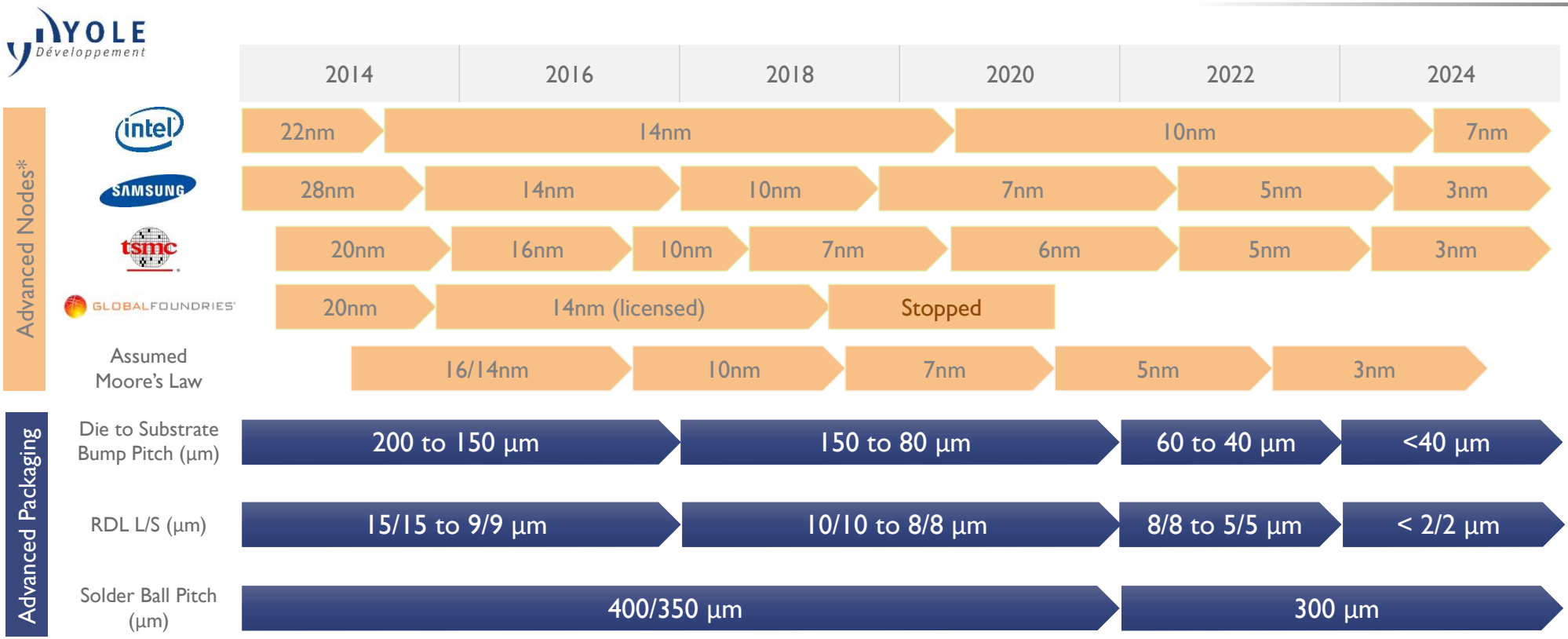
TECHNOLOGY ROADMAP: FROM NANO-SCALE TO MICRO-SCALE..



Industry is looking into the growing importance of functional roadmap

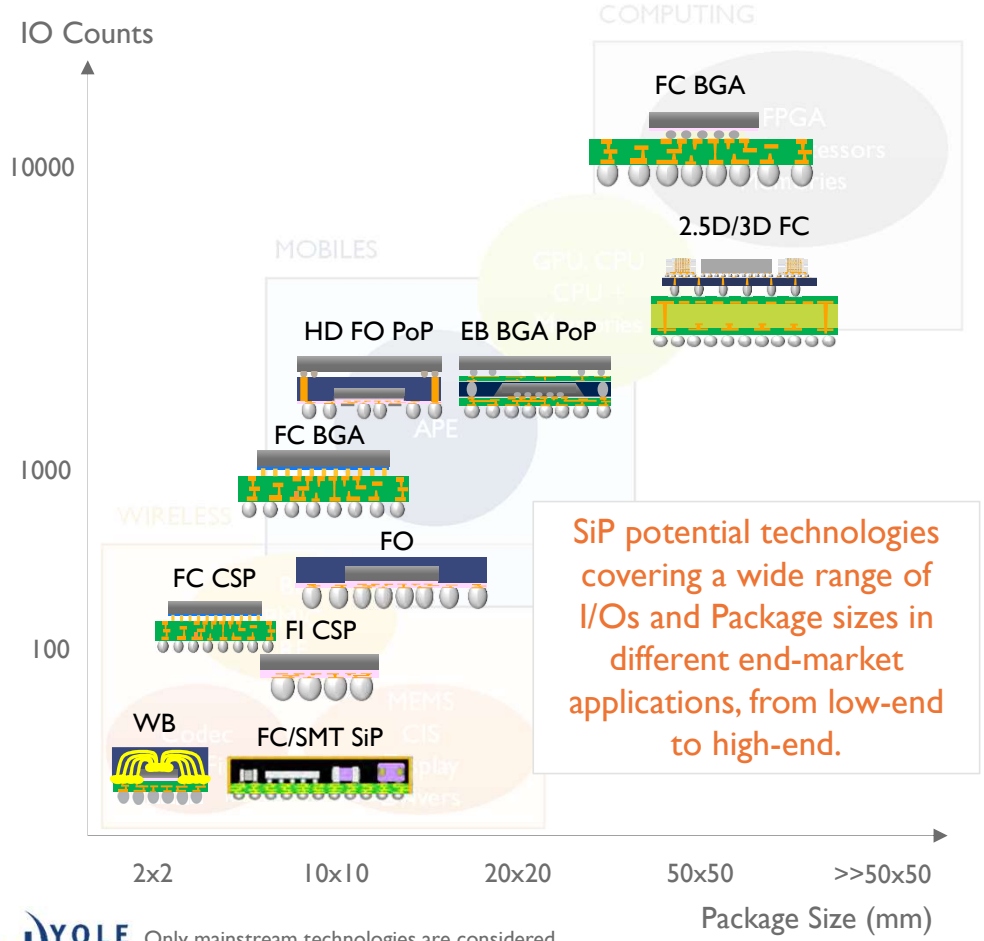
Advanced Packaging is required to bridge the scale-gap between Die and PCB

Non-exhaustive list of players listed

Average trends of the various industry players

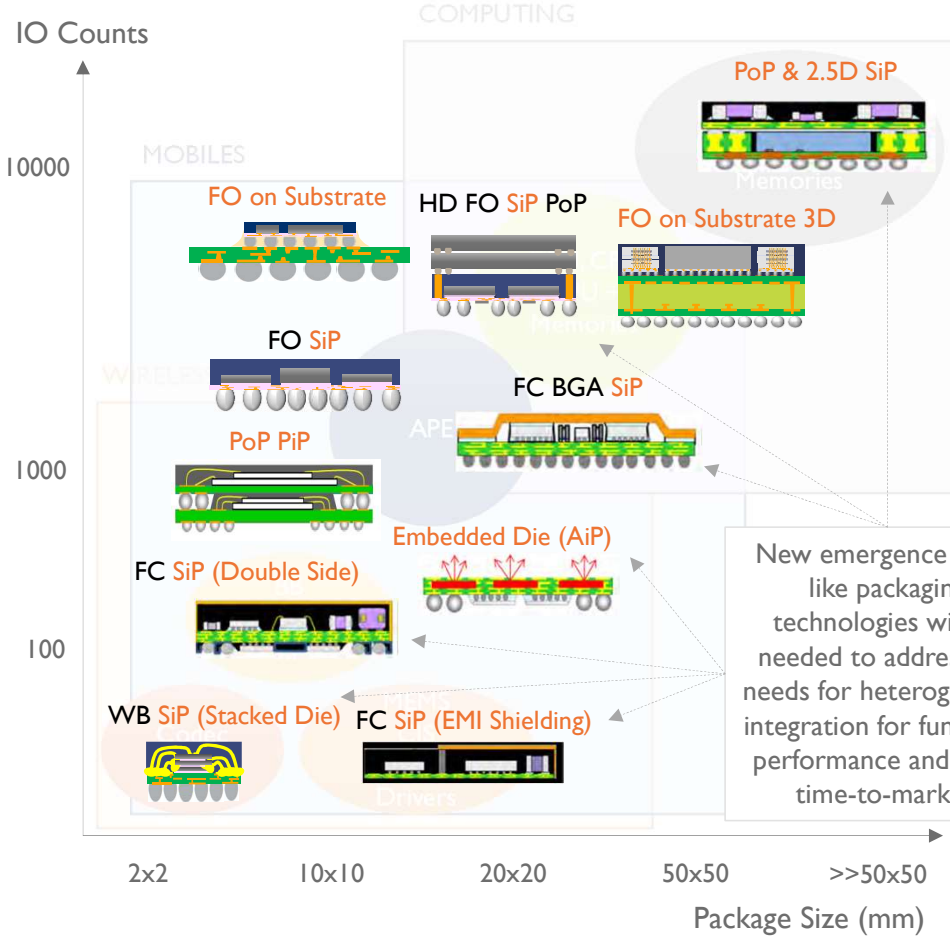
THE OLD AND THE NEW ADVANCED PACKAGING

< 2019 : Packaging Technologies



SiP potential technologies covering a wide range of I/Os and Package sizes in different end-market applications, from low-end to high-end.

2019 - 2030 : New capabilities needed for multi-die solution



New emergence of SiP like packaging technologies will be needed to address the needs for heterogeneous integration for functional performance and faster time-to-market.

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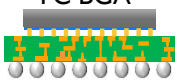
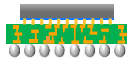
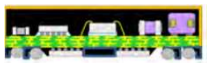
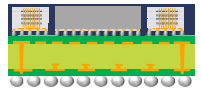
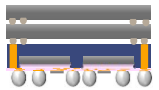
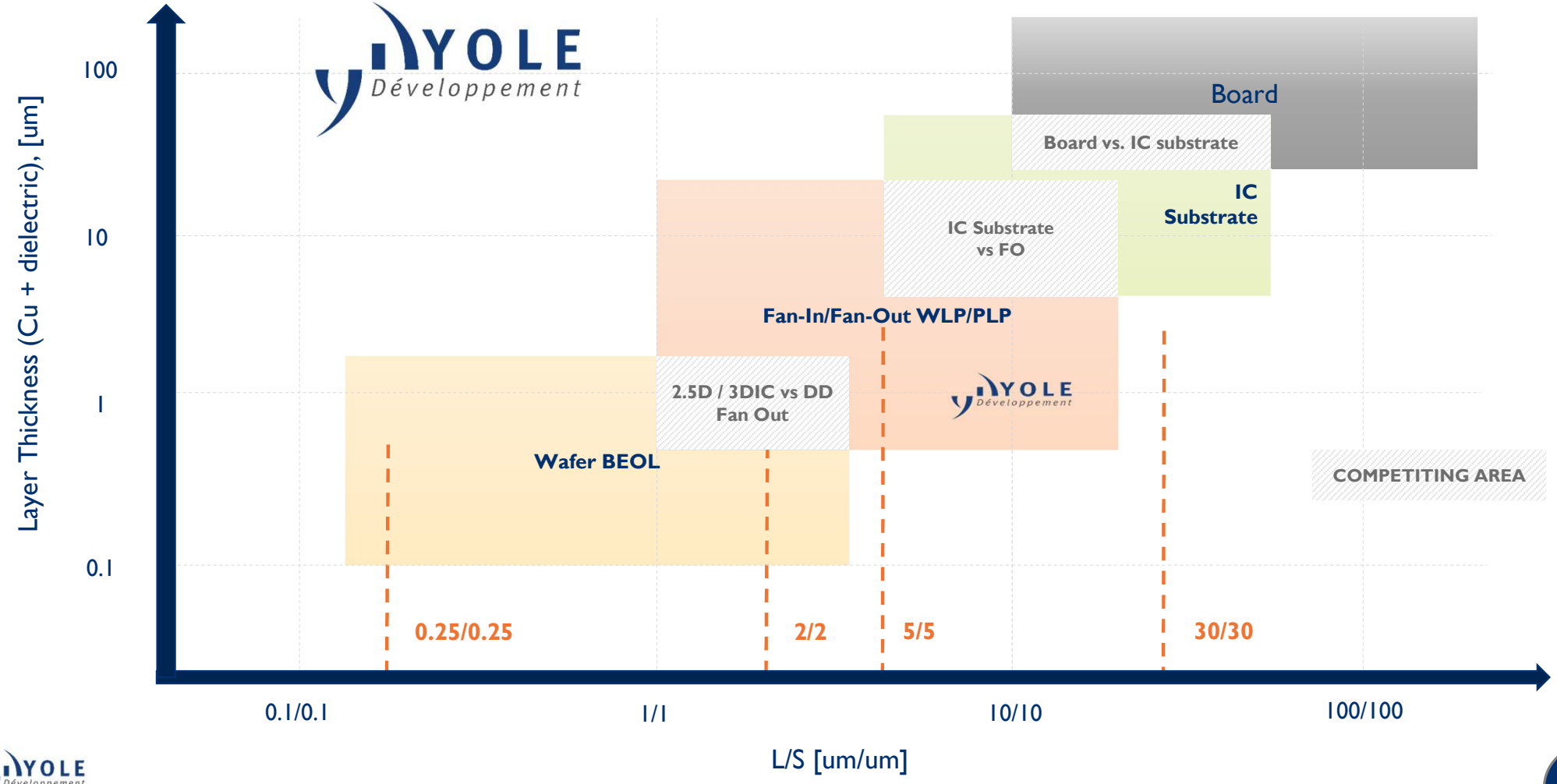
SIP TECHNOLOGY ROADMAPS: KEY PARAMETERS

Typical		Metrics	<2017	2019	2022	2025	SiP Advancement
Flip Chip (IC Substrate)	FC BGA  FC CSP 	Substrate RDL L/S	30/30 to 10/10 µm	8/8 to 5/5 µm		> 2/2 µm	FC BGA SiP 
		Substrate I/O Pitch	1200 to 350 µm			300 µm	
		Substrate I/O Ball	500 - 3000		>> 3000		
		Max Package Size	> 65x65 mm		>> 80x80 mm		Double Sided FC SiP 
		Max no. of Dies/Passives	< 15	< 35	>> 35		
		Max level of RDLs	10 -16x RDL		>> 10x RDL		
Fan-Out	FO 	Substrate RDL L/S	15/15 to 8/8 µm	5/5 µm to 2/2 µm		< 1/1 µm	FO on Substrate 
		Substrate I/O Pitch	400 µm	350 µm	200 µm		
		Substrate I/O Ball	< 300	600 -1300	>> 1500		
		Max Package Size	< 5x5 mm	< 25x25 mm		< 30x30 mm	HD FO SiP PoP 
		Max no. of Dies/Passives	≤ 2	≤ 4	≤ 6		
		Max level of RDLs	3x – 4x RDL		> 4x RDL		
Embedded Die	Embedded Passives 	Substrate RDL L/S	> 25/25 µm	> 20/20 µm		> 15/15 µm	Embedded Interconnects 
		Die I/O Pitch	250-80µm		50 µm		
		Die I/O Numbers	40-100	100-150		150-200	
		Max Package Size	<15x15 mm		< 25x25 mm		Embedded Multi-Dies 
		Max no. of Dies/Passives	≤ 2	≤ 3		≤ 4	
		Max level of RDLs	2x - 4x RDL		4x – 6x RDL		

Roadmap described here based on an expected average of the different technologies in the market.

ADVANCED PACKAGING TECHNOLOGY – FUTURE



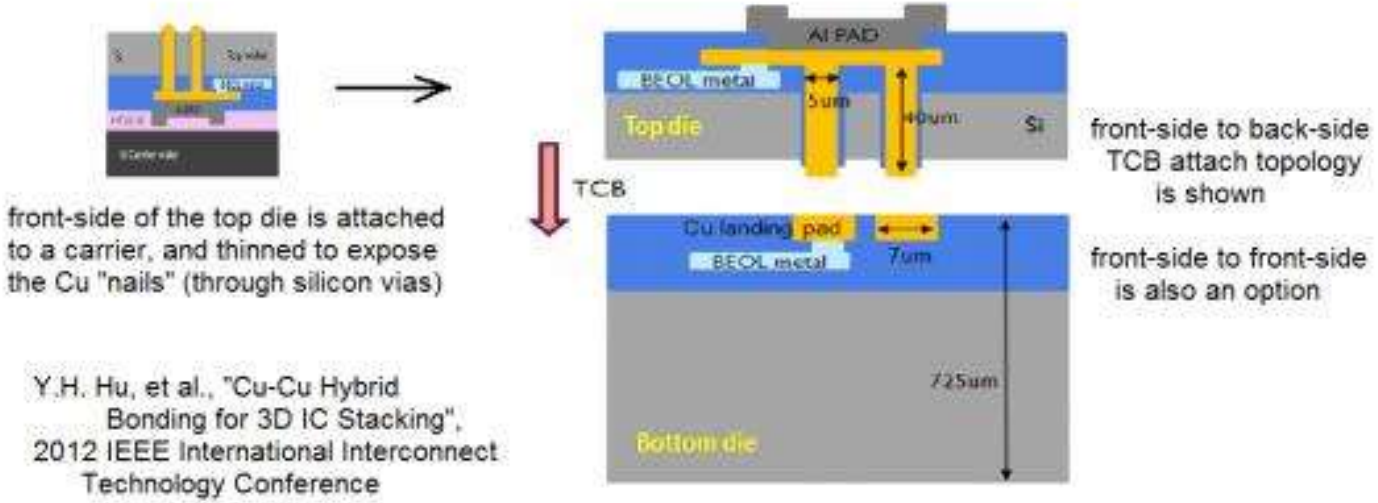
TSMC SOIC

System-on-Integrated-Chips (SoIC)

- TSMC announced the SoIC advanced packaging technology, that is slated to go into mass production in 2021.
  - SoIC is a "front-end" integration solution – "One stop shop"

TSMC emerged as the leader in developing innovative advanced packaging platform from fan-out to 3D IC packaging

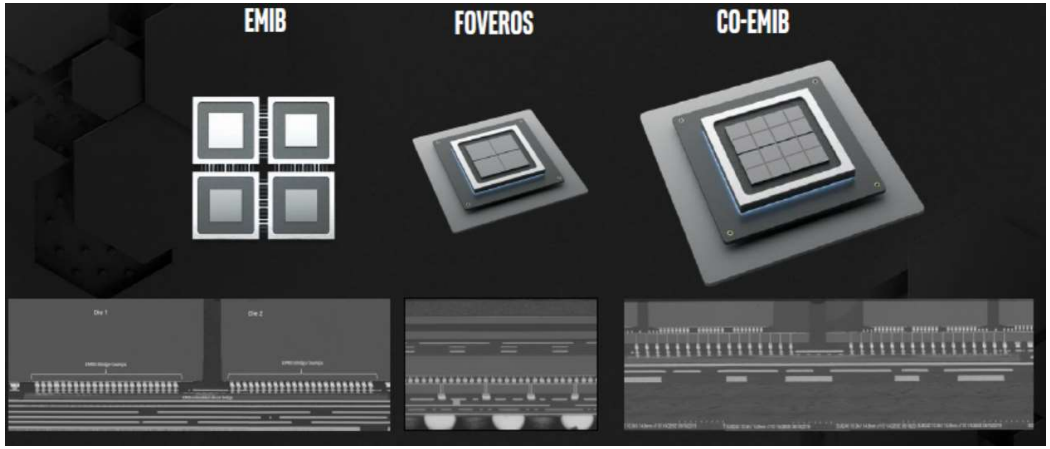
Thermo-compression bonding ("bumpless") for TSMC SoIC 3D stacking

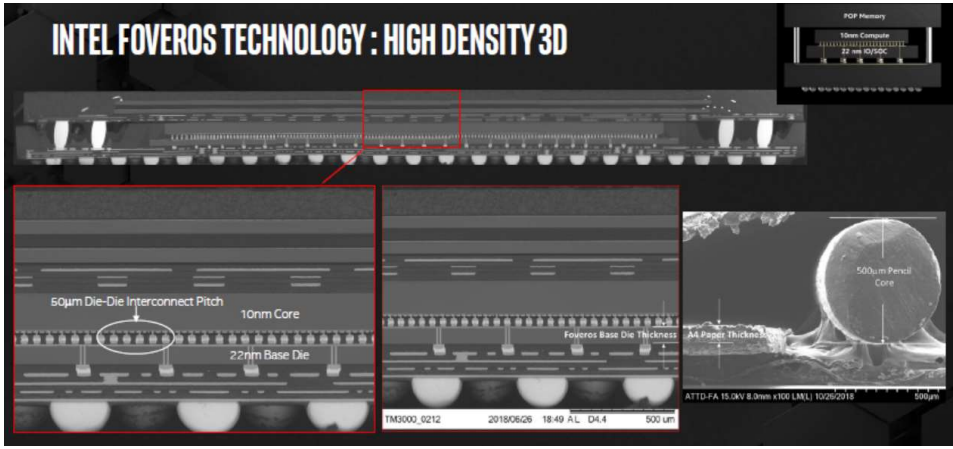


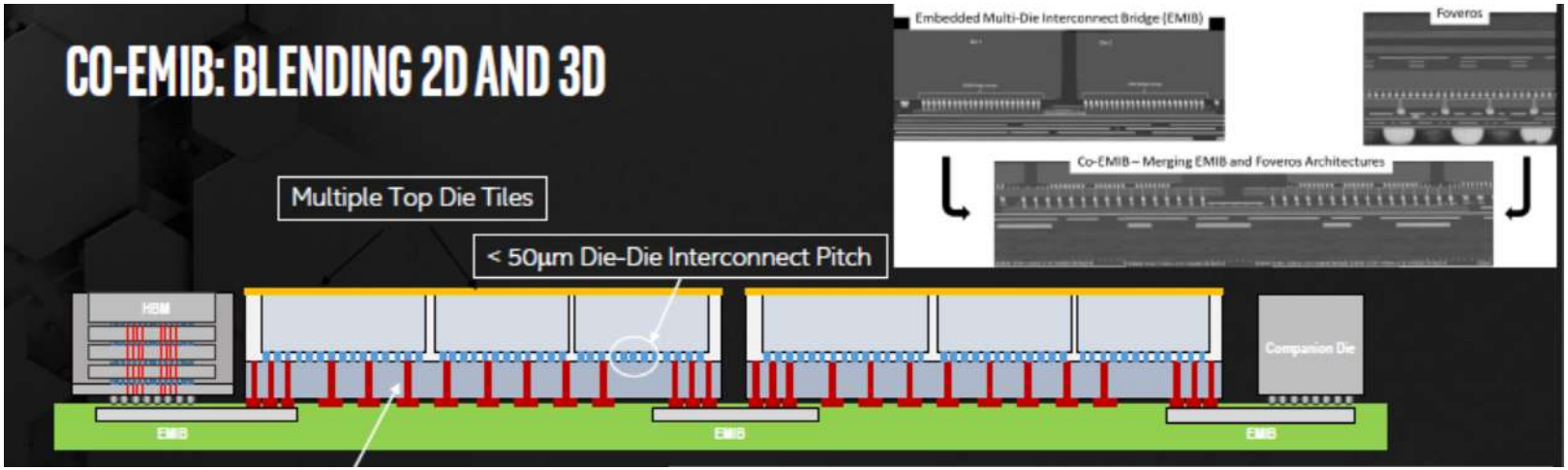
front-side of the top die is attached to a carrier, and thinned to expose the Cu "nails" (through silicon vias)

Y.H. Hu, et al., "Cu-Cu Hybrid Bonding for 3D IC Stacking", 2012 IEEE International Interconnect Technology Conference

INTEL'S "OMNIDIRECTIONAL" INTERCONNECTED FUTURE…

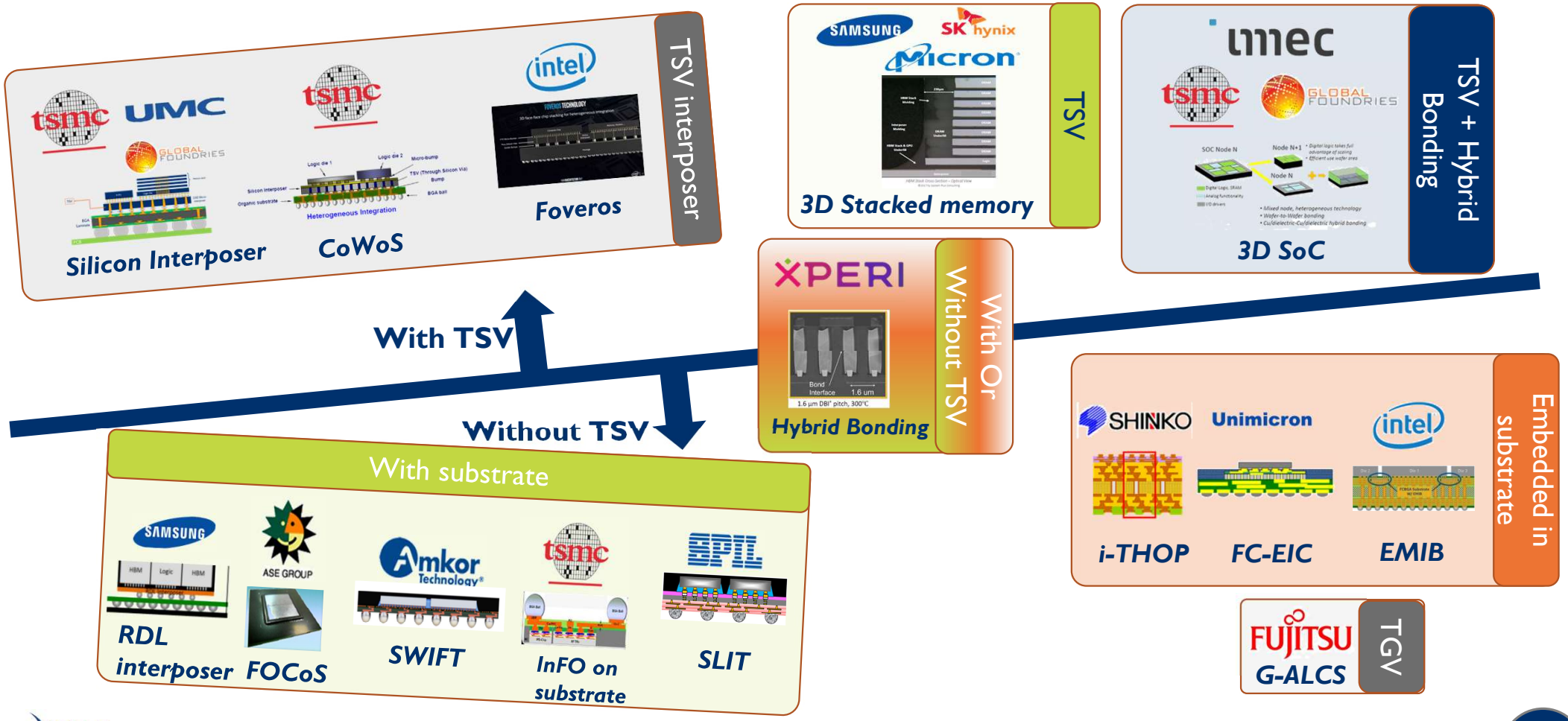






Source: Intel

2.5D & 3D STACKING TECHNOLOGIES

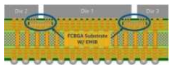


ALTERNATIVE TSV LESS TECHNOLOGY

Several players developing alternative technologies to TSV Si interposer

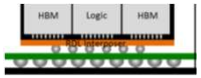
ALTERNATIVE TECHNOLOGIES to TSV interposer

EMIB



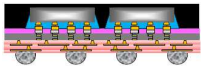
Silicon bridge instead of Si TSV interposer

RDL interposer



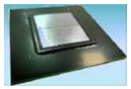
RDL interposer instead of Si TSV interposer

SLIT



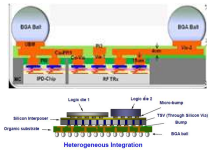
0µm Silicon

FOCoS



RDL deposition & etching + flip chip

InFO on substrate & CoWoS

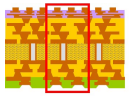


- RDL deposition & etching + flip chip
- Heterogeneous integration on interposer

SWIFT

Chip last + RDL deposition & etching

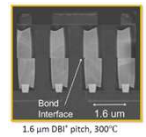
Embedded trace



i-THOP *FC-EIC*

Embedded metal layers or embedded Si interposer

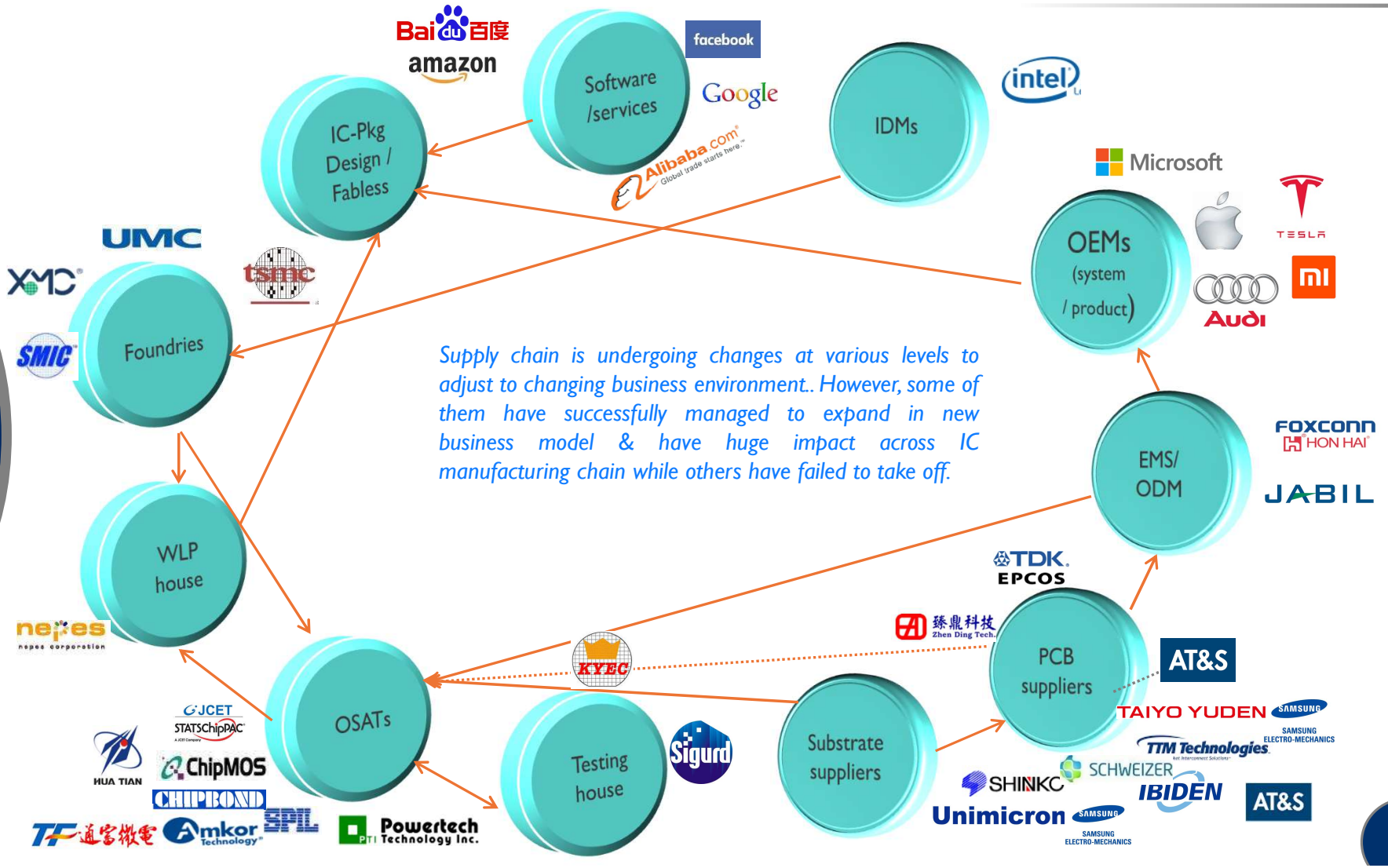
Hybrid Bonding



2 wafers bonding with Cu bumps. No TSV needed

SEMICONDUCTOR SUPPLY CHAIN UNDERGOING CHANGE AT VARIOUS LEVELS

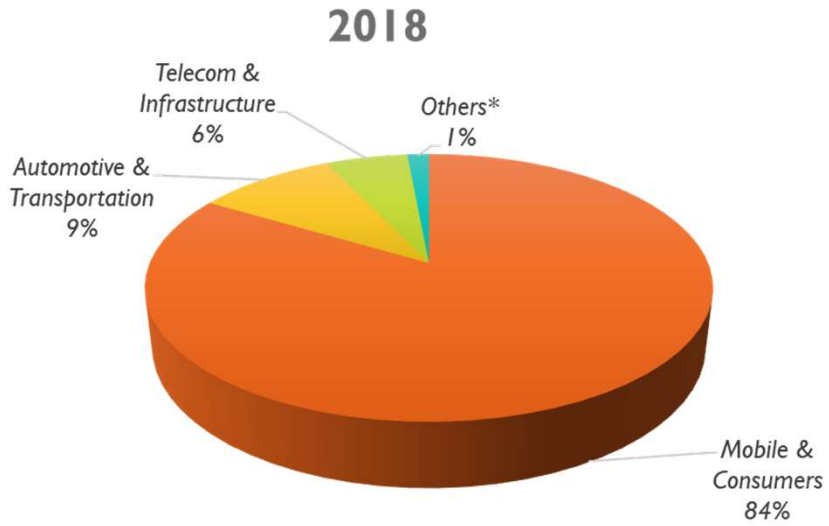
In order to expand the business and explore new areas, players in semiconductor supply chains are moving to different business models

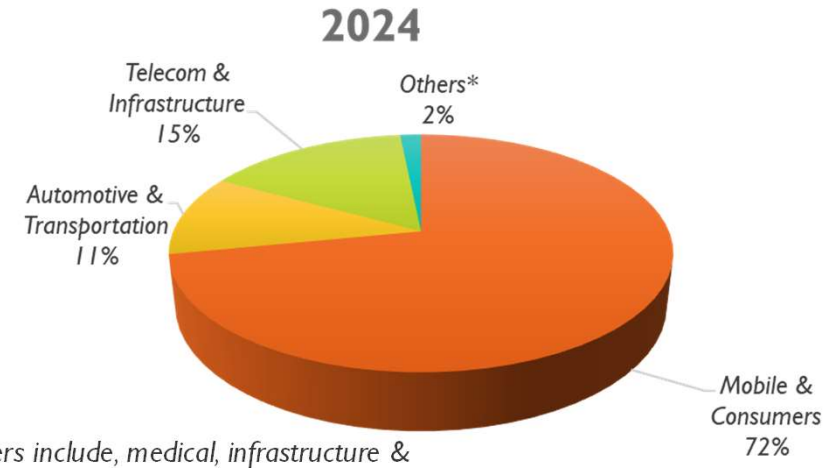


Supply chain is undergoing changes at various levels to adjust to changing business environment.. However, some of them have successfully managed to expand in new business model & have huge impact across IC manufacturing chain while others have failed to take off.

ADVANCED PACKAGING REVENUE FORECAST: BREAKDOWN BY APPLICATIONS

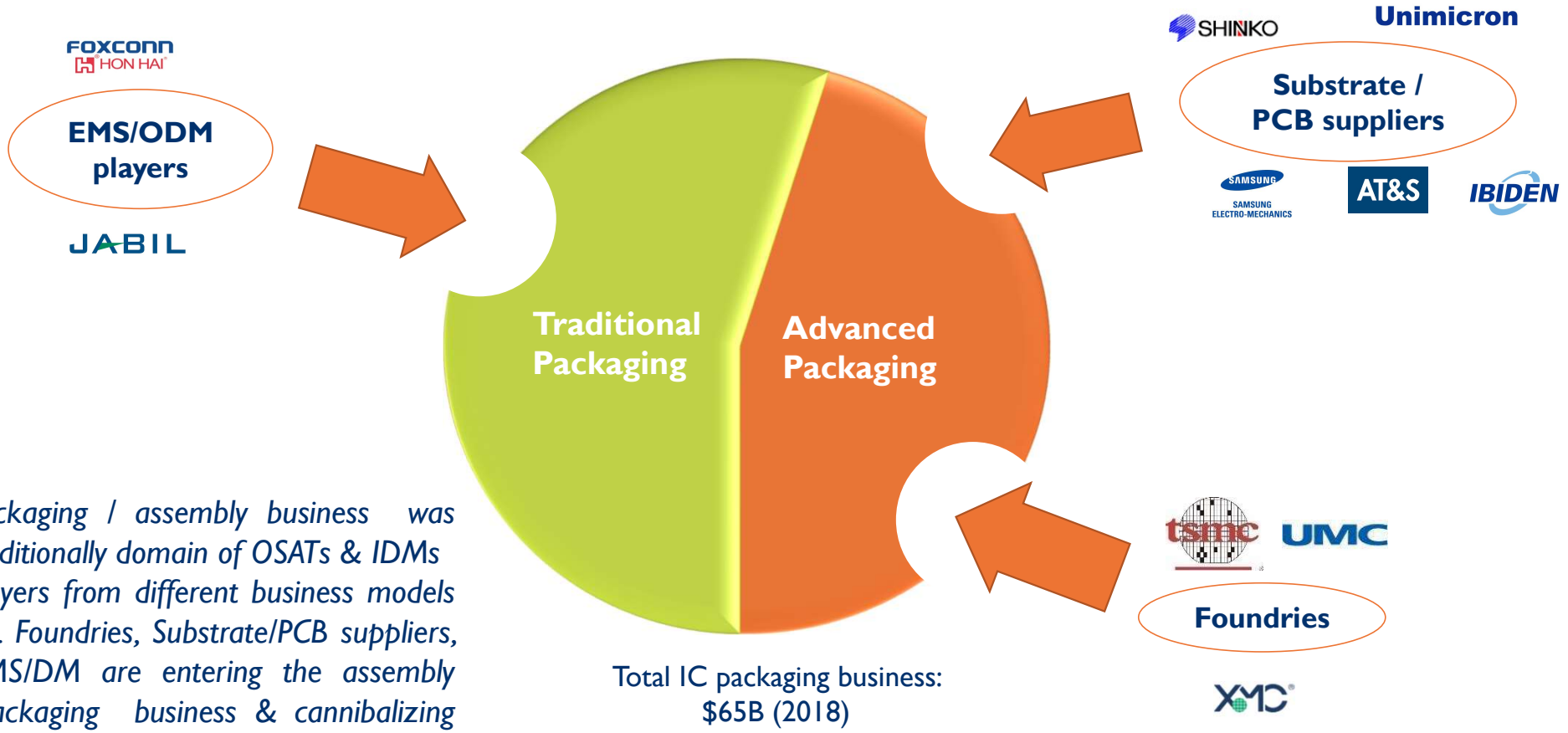
Mobile & Consumer	**CAGR (2018-2024) ~ 5%**
Automotive & Transportation	**CAGR (2018-2024) ~ 11%**
Telecom & Infrastructure	**CAGR (2018-2024) ~ 28%**
*Others**	**CAGR (2018-2024) ~ 9%**





* Others include, medical, infrastructure & aerospace/defense segments

OSATS PACKAGING BUSINESS CANNIBALIZATION TREND

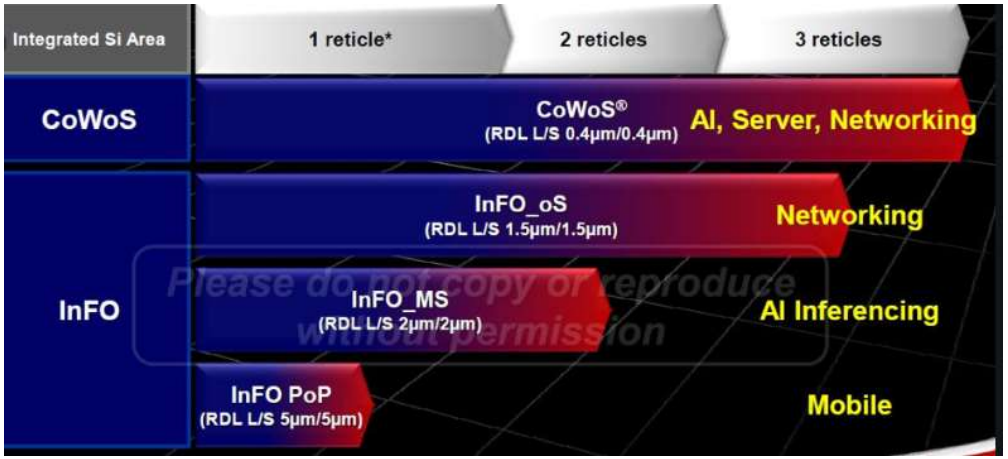


- *Packaging / assembly business was traditionally domain of OSATs & IDMs*
- *Players from different business models viz. Foundries, Substrate/PCB suppliers, EMS/DM are entering the assembly /packaging business & cannibalizing the OSAT business*

Total IC packaging business: $65B (2018)

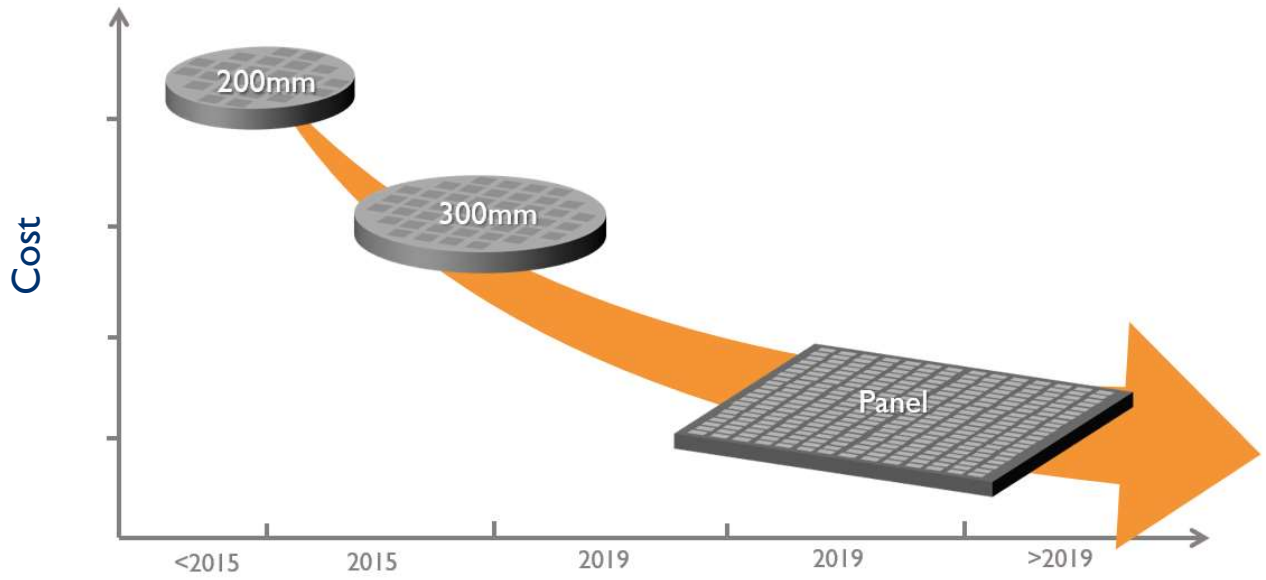
FAN-OUT PORTFOLIO: AN ENABLER FOR 3D IC INTEGRATION…

ASE , TSMC, JCET, PTI & SAMSUNG TO WATCH FOR ON NEW FO PLATFORMS FOR YEARS TO COME…



PANEL LEVEL FAN-OUT IS ALMOST HERE…..

Panel Level Fan-out



- ASE, PTI, Samsung and Nepes remain key panel level drivers
- Suppliers are putting capabilities in place, but high volume is yet to be achieved
- Suppliers streamlining panel size (e.g. 600 x 600)
- PTI investing significant CapEx in panel line for 3D IC mfg

WHAT TO EXPECT IN NEXT FIVE YEARS IN ADVANCED PACKAGING?

Increased Device Integration trend continues

- AP to memory
- RF modules / complex SMT devices /higher number of SMT passives
- AiP Modules

OSATs continue to up-level their capabilities in terms of new process/ equipment /material development to support thinner, denser and integrated IC packages

Some level of M&A for niche technology /process (Few players left to support scale & complexity)

Foundry/IDM players such as TSMC, Intel, and Samsung to invest in 3D IC package architectures

Cost will continue to be a driver as smartphone demand saturates – Increased performance at same or slightly higher price

5G, AI, and IoT to remain key megatrends to fuel growth in next 5 years

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Thank you for your attention!

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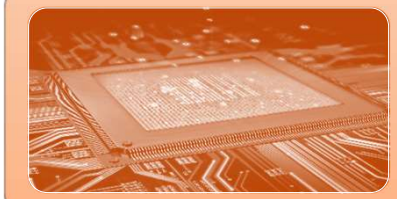
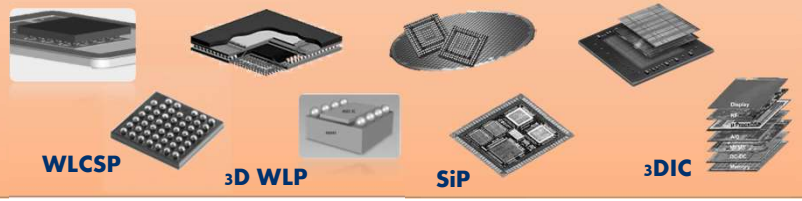
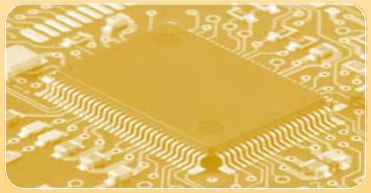


ADVANCED PACKAGING

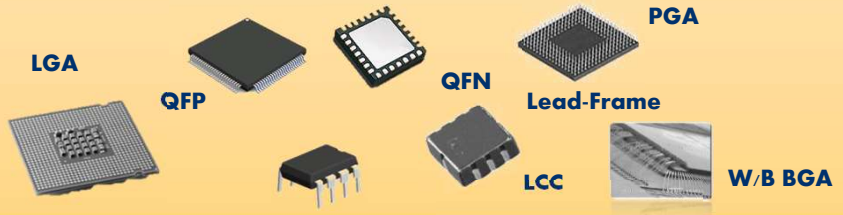
- Fan Out Packaging - PoP
- 3D / 2.5D Packaging - SiP
- Flip Chip BGA
- WLCSP

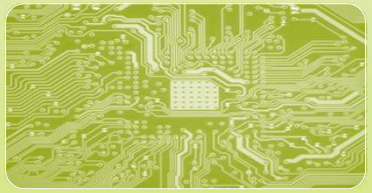




PACKAGING

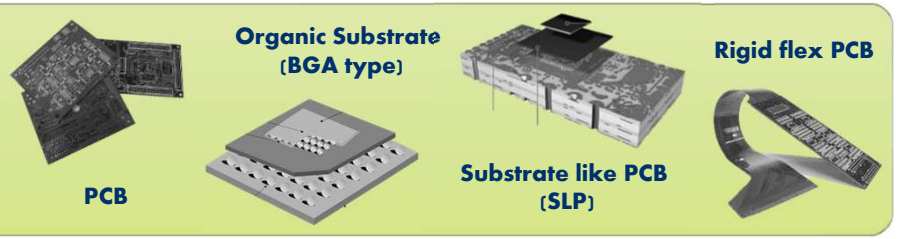
- Leadframe packages
- Ceramic packages





SUBSTRATES

- Advanced Substrates
- Printed Circuit Board
- Embedded Dies
- Substrate like PCB (SLP)



APPLICATIVE PACKAGING

- CMOS Image Sensor
- MEMS & Sensors
- Power & LED
- Photonics