

Package Assembly Design Kits

What are they and how they can benefit the packaging community

John Park

Advanced IC Packaging and Cross-Platform Solutions

000544

Outline



Market Trends

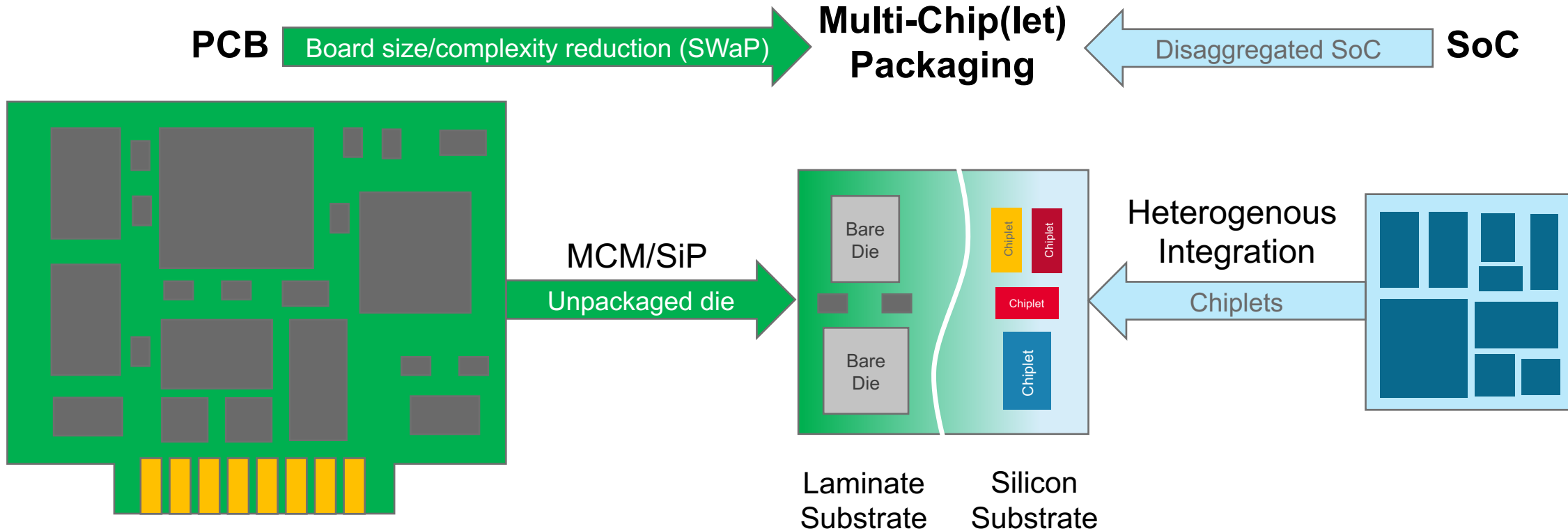
History and purpose of a PDK

Why it's time for PDK-like solution for package designers

Contents of an Assembly Design Kit (ADK)

Chiplet-Based (Heterogeneous Integration) Architectures

The transition from system on a chip (SoC) to system in a package (SiP)



PCB to MCM/SiP Benefits

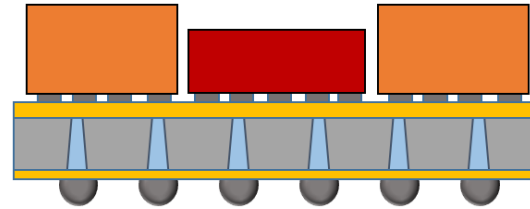
Smaller footprint
PCB simplification
Higher bandwidth
Lower power

SoC to HI Benefits

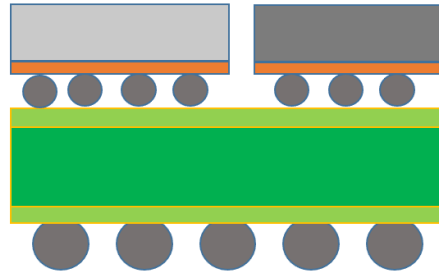
Reduced NRE costs
Shorter time to market
Larger than reticle size designs
More flexible architectures

Packaging Technologies Being Targeted for Heterogenous Integration

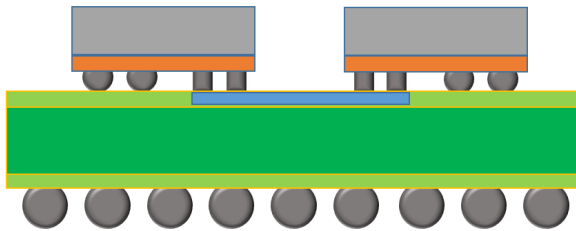
Silicon
Interposers
(2.5D-IC)



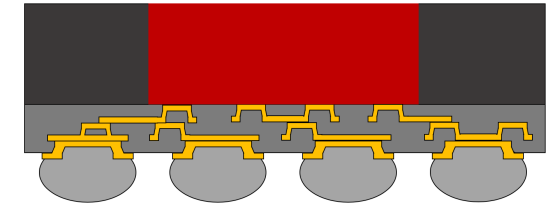
Laminate
BGA/LGA



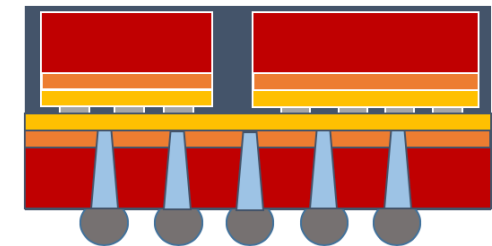
Embedded
Bridges



High-
Density
RDL
(FOWLP)



Chip-on-
Wafer
Stacking
(3D-IC)



Outline



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Contents of an Assembly Design Kit (ADK)

History and Purpose of a Process Design Kit (PDK)

- The original concept of PDK (Process Delivery Kit) came out of Texas Instruments in January of 1991 with a goal of providing IC designers with everything they need to know, based on the manufacturing process, to design their chip. And to deliver this knowledge through EDA design tools/flows
 - In other words...to connect the manufacturing process with the design process
 - Cadence adopted the concept and renamed the term PDK to Process Design Kit (PDK) in 1993

Paul Koch – Retired Semiconductor Executive



Outline



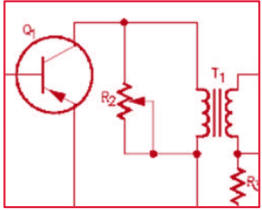
Market Trends

History and purpose of a PDK

Why it's time for PDK-like solution for package designers

Contents of an Assembly Design Kit (ADK)

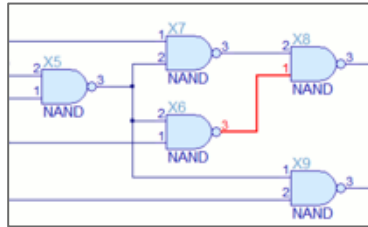
Design and Verification is Only Getting Harder



Transistor-level

1980

Functional

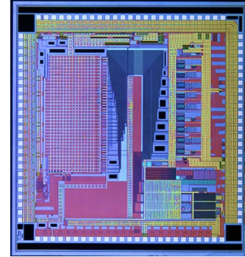


Gate-level

1990

Functional

Timing



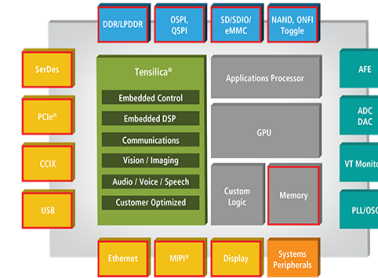
ASIC

2000

Functional

Timing

Power



SoC

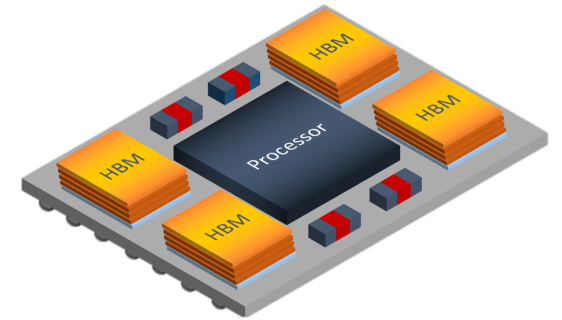
2010

Functional

Timing

Power

Reliability



Heterogeneous Integration

Now

Functional

Timing

Power

Reliability

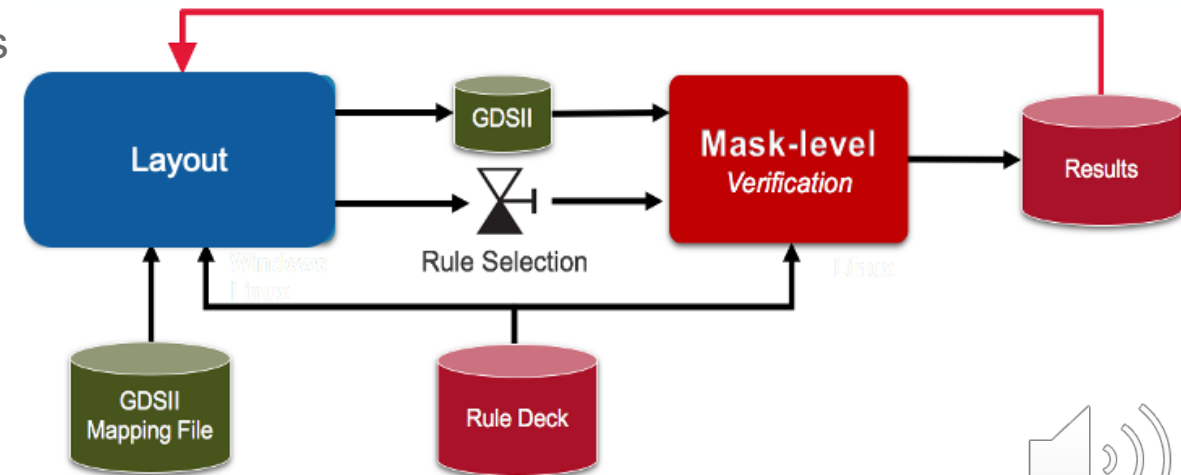
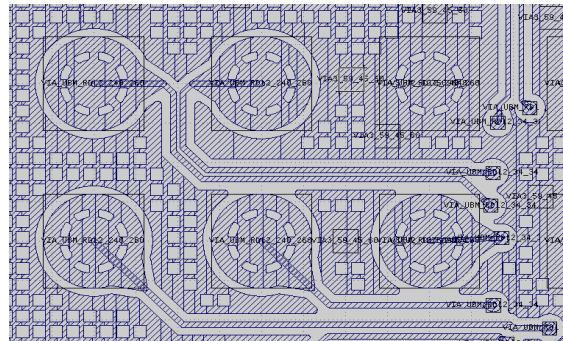
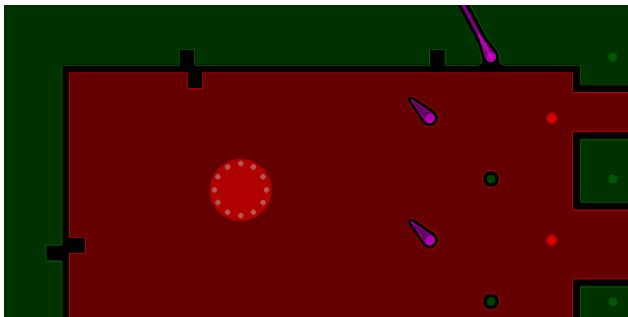
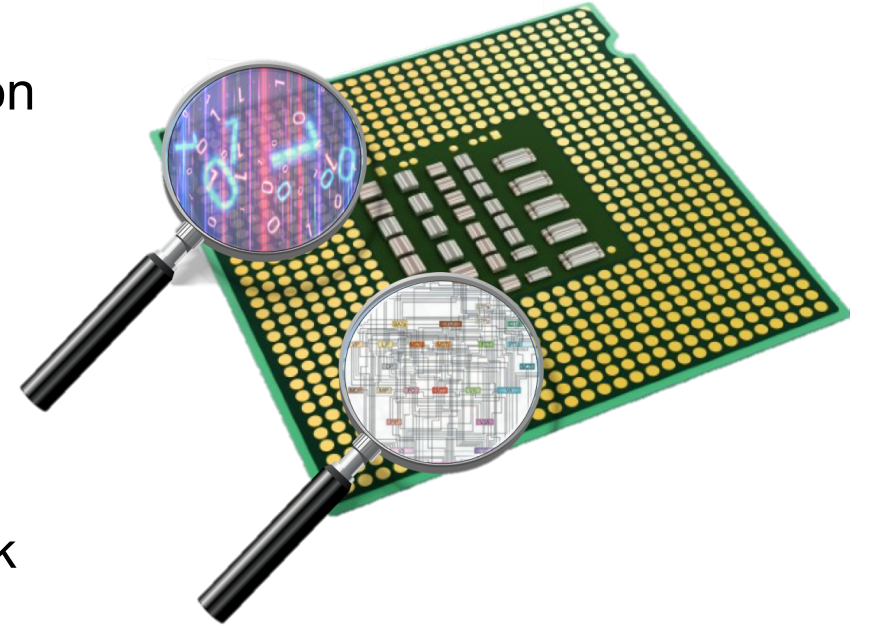
System-Level

Thermal

Mechanical

Design Tool/Flow Challenges for the Package Design Team

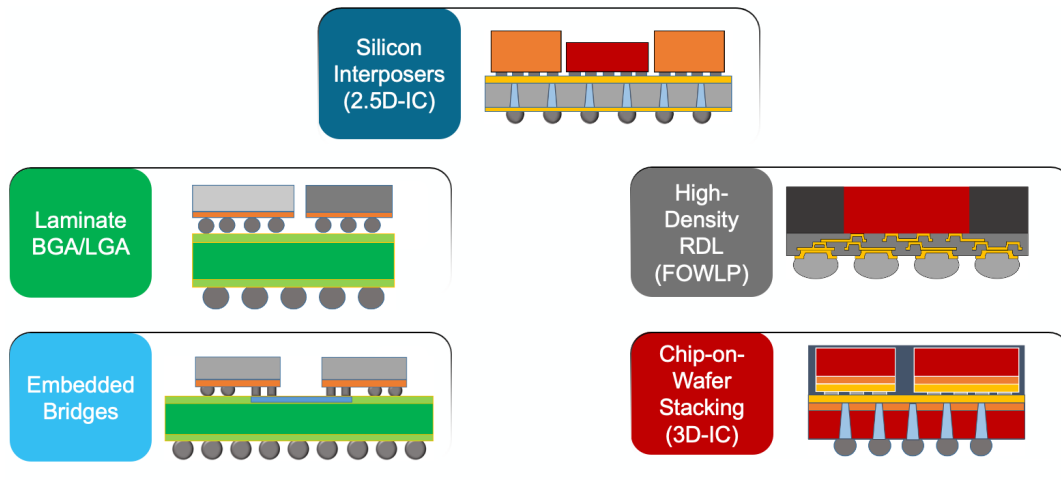
- Advanced multi-chip(let) silicon-based packages require specialized layout features and formal physical/logical verification capabilities
- Layout features specific to silicon substrate designs
 - Advanced filleting and trace widening
 - Progressive shape and pad degassing algorithms
 - High-capacity design support
- Mask-level accurate output data (GDSII) from substrate layout tool
 - Advanced arc vectorization
- Seamless integration with IC physical verification tool with feedback loop to layout
 1. Mask-level DRC
 2. Connectivity verification (LVS) of multi-chip(let) designs
 3. Region specific advanced metal fill (balancing)



Why We Need ADKs



It's time for package designers to stop guessing and start knowing



IC designers are new to packaging and package designers are new to IC/silicon substrates

Outline



Market Trends

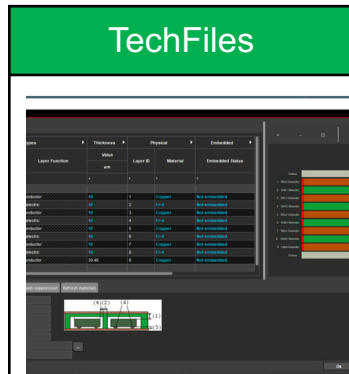
History and purpose of a PDK

Why it's time for PDK-like solution for package designers

Contents of an Assembly Design Kit (ADK)

(Package) Assembly Design Kit (ADK)

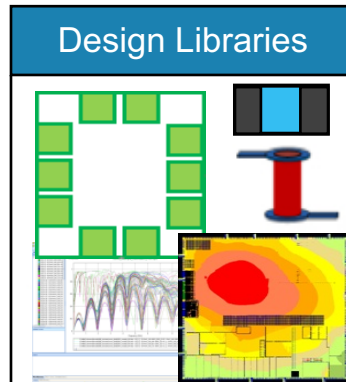
- Looking Beyond Design-Rule Manuals and Reference Designs...



Layer stack-up

Material
Properties
Thickness

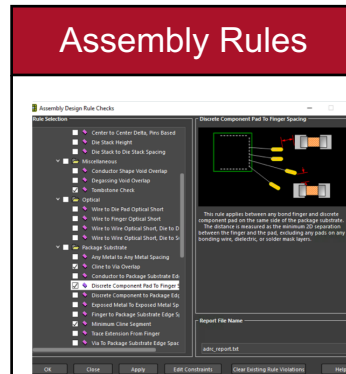
Physical/Electrical
layout constraints



Footprints

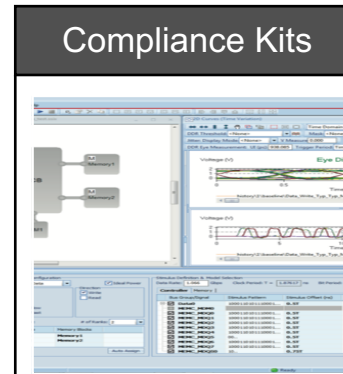
Discrete
BGA/LGA
3D Mechanical

Bond-Wire profiles
IO models
Thermal models
Power models



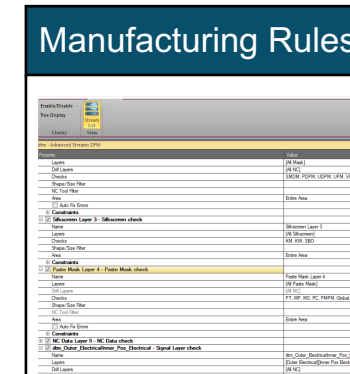
Device placement constraints based on assembly pick & place equipment

Die to die spacing
Device to device
Device to obstacle



Electrical spec validation of chip(let)-to-chip(let) interfaces

Jitter tolerance
Insertion loss
Return loss
Eye mask



Board/substrate manufacturing process

Substrate checks
Soldermask checks
Soldering issues
Silkscreen checks



Foundry/semiconductor manufacturing process

DRC
LVS
Metal fill

Tech File

- ASCII file
 - Easy to manage and share
- Read, write and compare
- Re-use
- Contents
 - Substrate stack-up physical and electrical details
 - Physical/Spacing signal constraints
 - Electrical signal constraints
 - Constraint groupings
 - Assembly/placement rules
 - Test rules

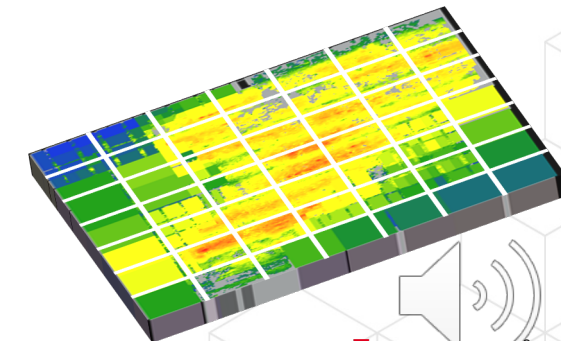
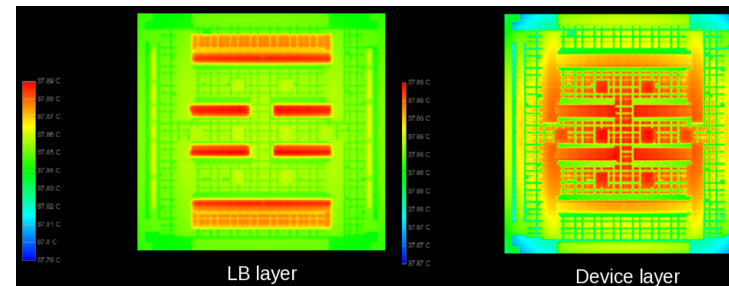
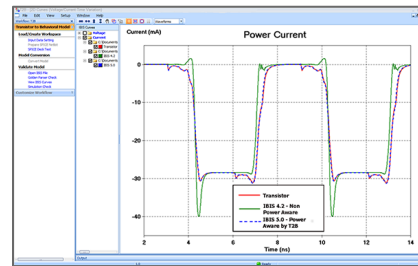
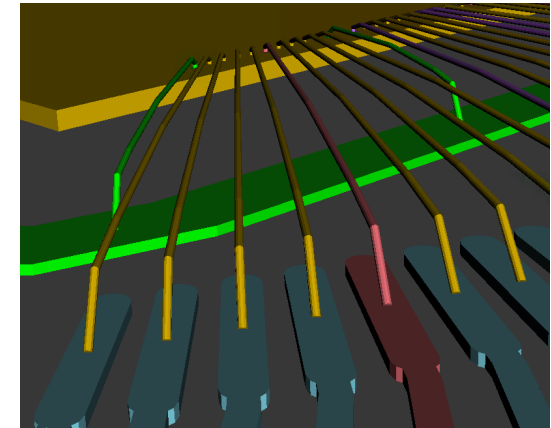
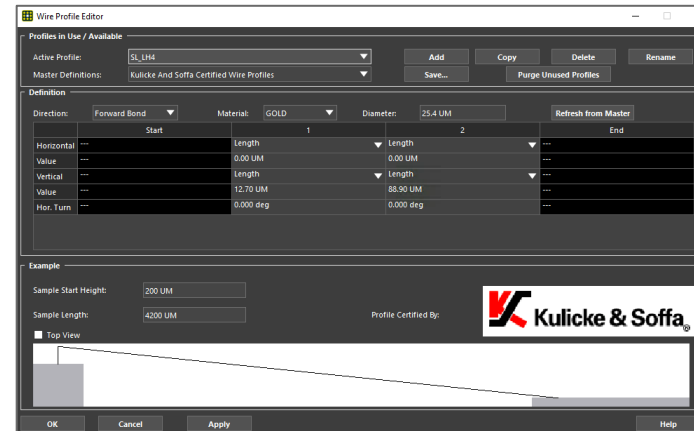
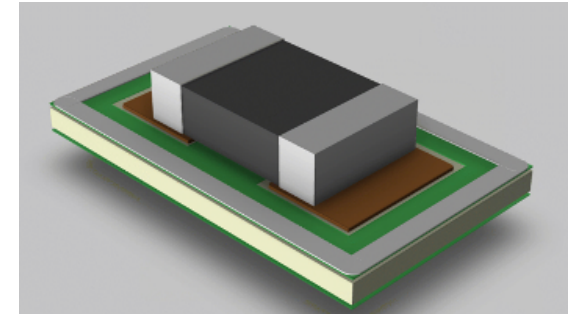
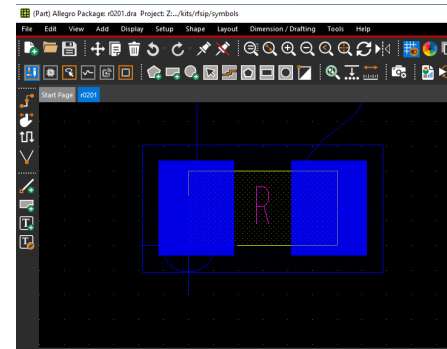
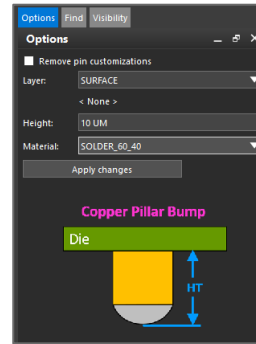
The screenshot displays the Cadence Cross-section Editor and the Physical Constraint Set dialog. The Cross-section Editor shows a stack-up of layers with a table of properties and a 3D cross-section view. The Physical Constraint Set dialog shows a table of constraints for various signal types.

Objects	Types	Thickness	Physical	Embedded			
#	Name	Layer	Layer Function	Value	Layer ID	Material	Embedded Status
				um			
1	RDL0	Conductor	Conductor	10	1	Copper	Not embedded
2	VIA01	Dielectric	Dielectric	10	2	Fr-4	Not embedded
3	RDL1	Conductor	Conductor	10	3	Copper	Not embedded
4	VIA12	Dielectric	Dielectric	10	4	Fr-4	Not embedded
5	RDL2	Conductor	Conductor	10	5	Copper	Not embedded
6	VIA23	Dielectric	Dielectric	10	6	Fr-4	Not embedded
7	RDL3	Conductor	Conductor	10	7	Copper	Not embedded
8	VIA30	Dielectric	Dielectric	10	8	Fr-4	Not embedded
9	UBM	Conductor	Conductor	30.48	9	Copper	Not embedded

Type	S	Name	Referenced Physical CSet	Min	Max	Min Width	Max Length
				um	um	um	um
Dsn		advwip_artwork_2	DEFAULT	40,000	0.000	40,000	0.000
DPr		DP_TXDATA0	DEFAULT	40,000	0.000	40,000	0.000
DPr		DP_TXDATA1	DEFAULT	40,000	0.000	40,000	0.000
DPr		DP_TXDATA2	DEFAULT	40,000	0.000	40,000	0.000
DPr		DP_TXDATA3	DEFAULT	40,000	0.000	40,000	0.000
DPr		DP_TXDATA4	DEFAULT	40,000	0.000	40,000	0.000
DPr		DP_TXDATA5	DEFAULT	40,000	0.000	40,000	0.000
DPr		DP_TXDATA6	DEFAULT	40,000	0.000	40,000	0.000
DPr		DP_TXDATA7	DEFAULT	40,000	0.000	40,000	0.000
DPr		RXDATA0	DEFAULT	50,000	0.000	30,000	0.000
DPr		RXDATA1	DEFAULT	50,000	0.000	30,000	0.000
DPr		RXDATA2	DEFAULT	50,000	0.000	30,000	0.000
DPr		RXDATA3	DEFAULT	50,000	0.000	30,000	0.000
DPr		RXDATA4	DEFAULT	50,000	0.000	30,000	0.000

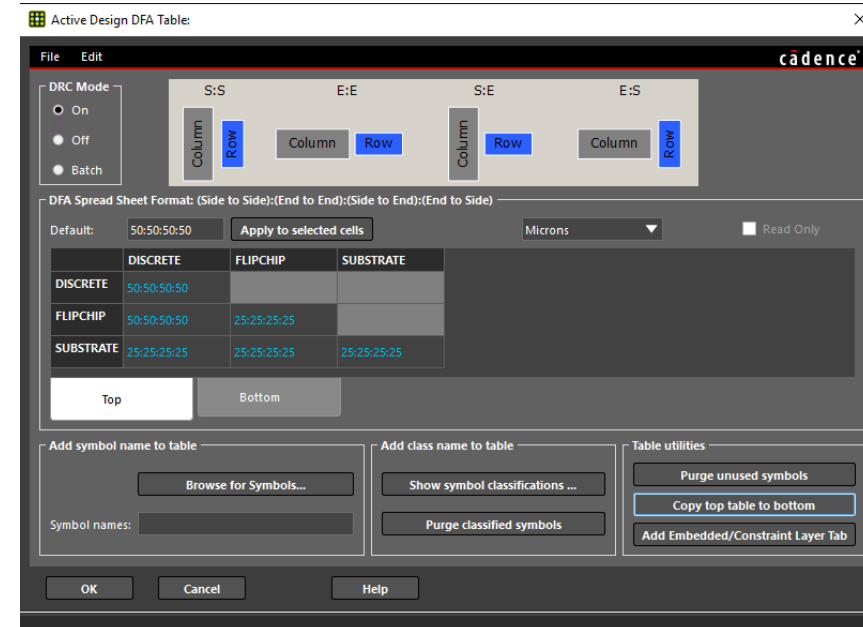
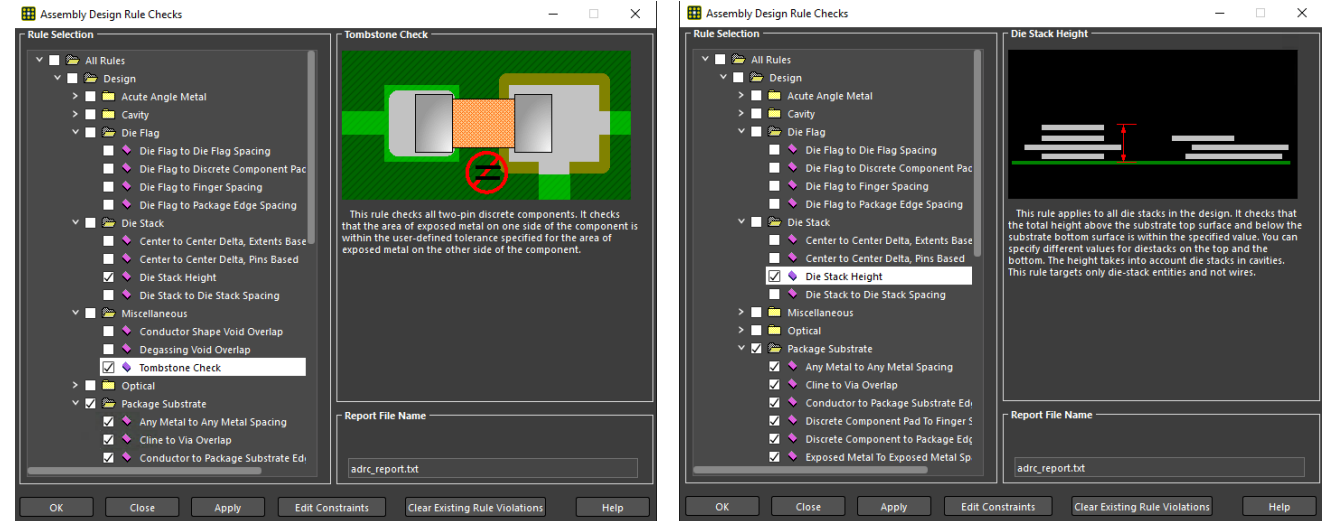
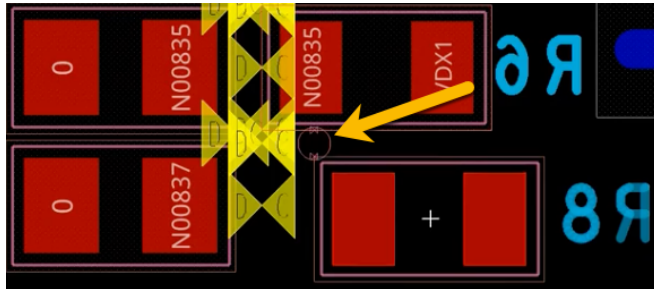
Design Libraries and Models

- Footprints
 - JEDEC standard BGA/LGA and SMD
 - Padstacks
 - STEP files (true 3D rendering)
- 3D Bond wire profiles
 - Model based on bonding equipment
 - Required for 3D DRC
- I/O models
 - Behavioral (IBIS)
 - Transistor-level
- Thermal/Power models
 - Chip(let)-level thermal and power models
 - Static and Transient Power information



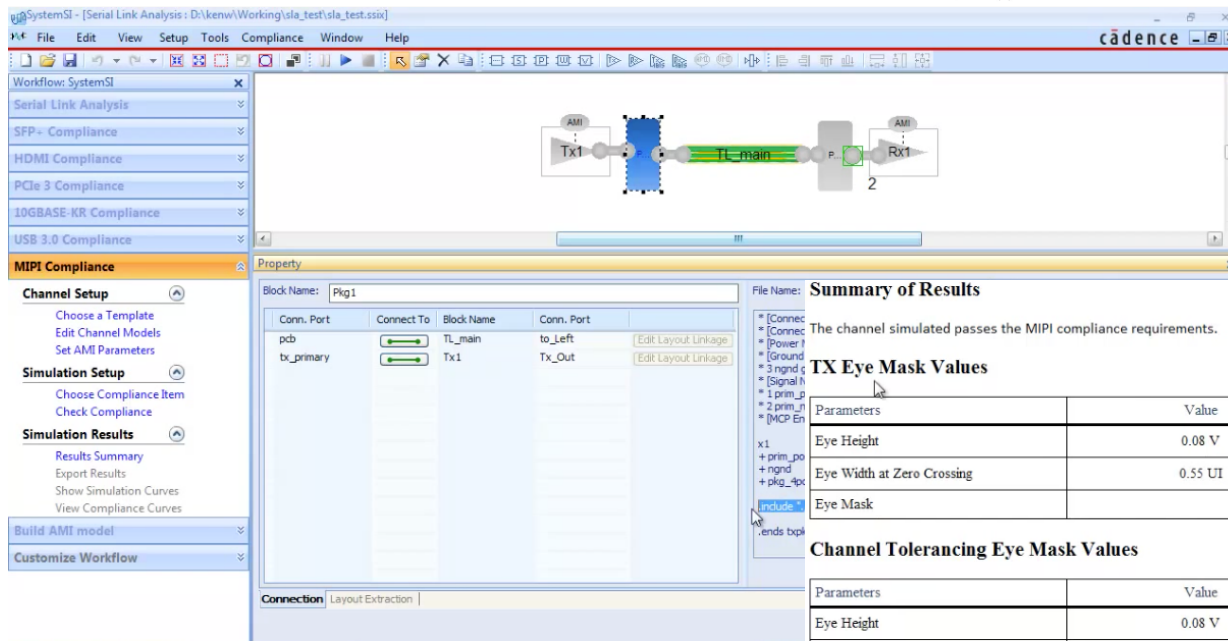
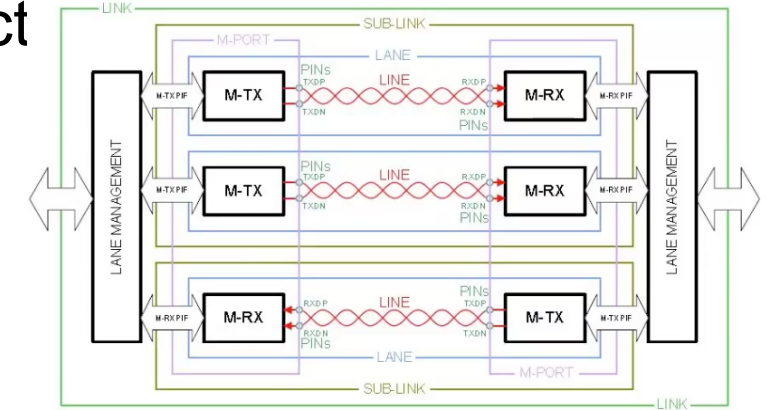
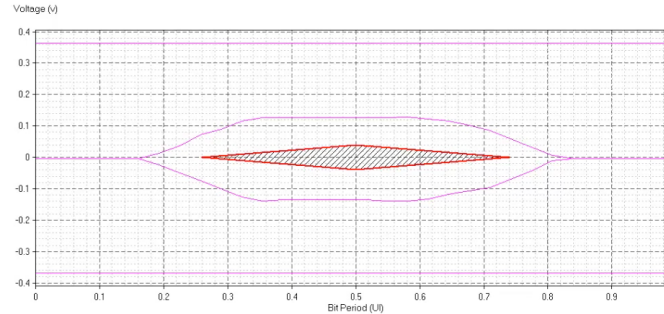
Design for Assembly

- GUI driven assistant to ease setup
- Unique to device DFA outline
- In-design direct feedback during component placement and move
- Table-driven with user defined component categories
- Basic mode (table) and advanced mode (Constraint Manager)
- Rule definition setup can be done in separate tool at the library level



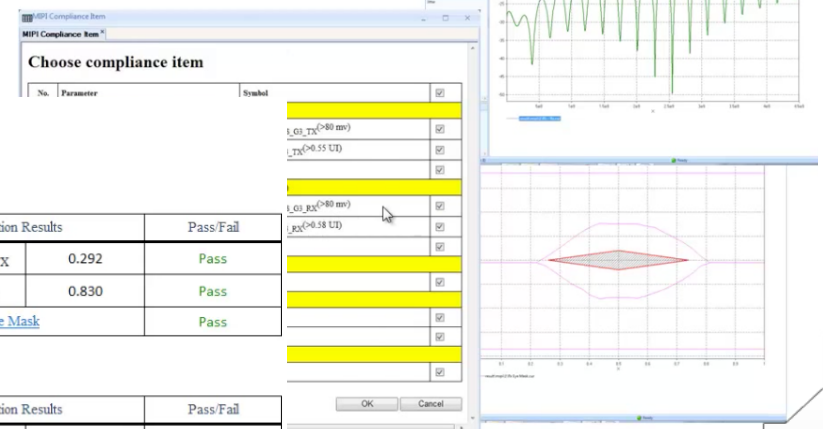
Compliance Kits

- Electrical validation of chip(let)-to-chip(let) interconnect



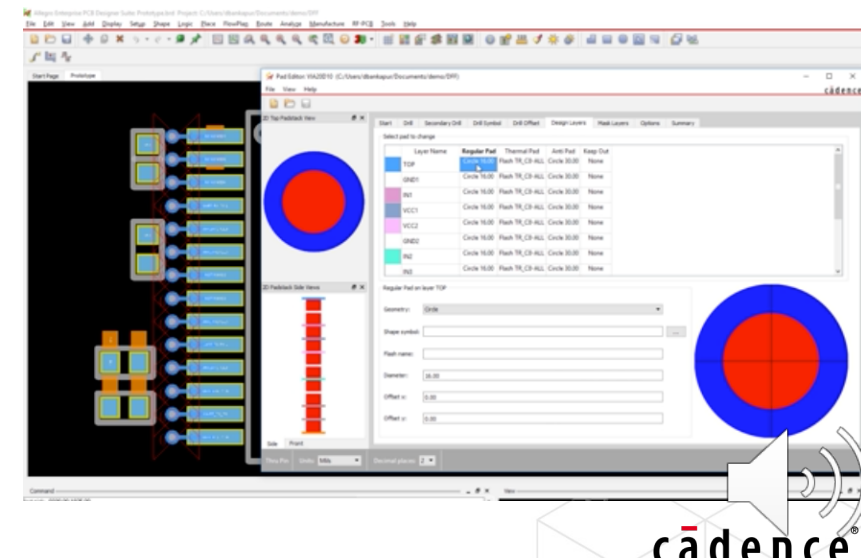
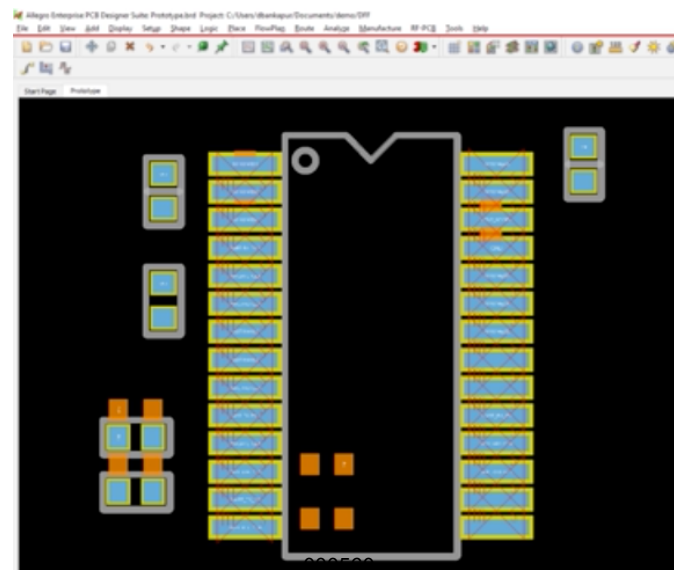
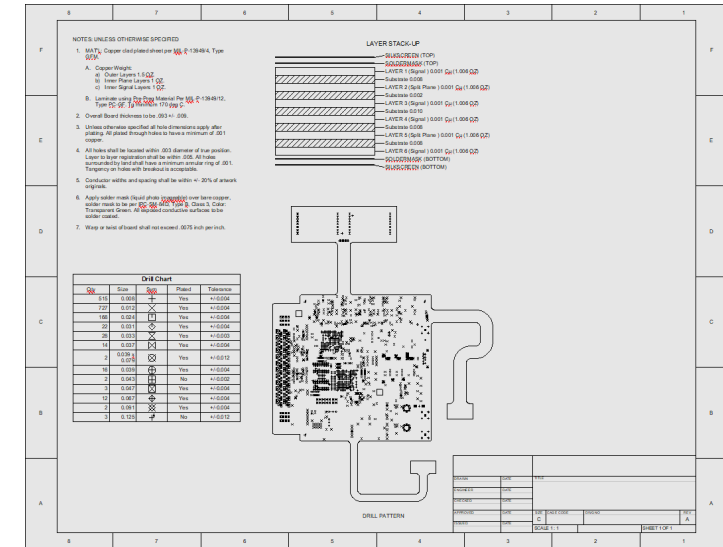
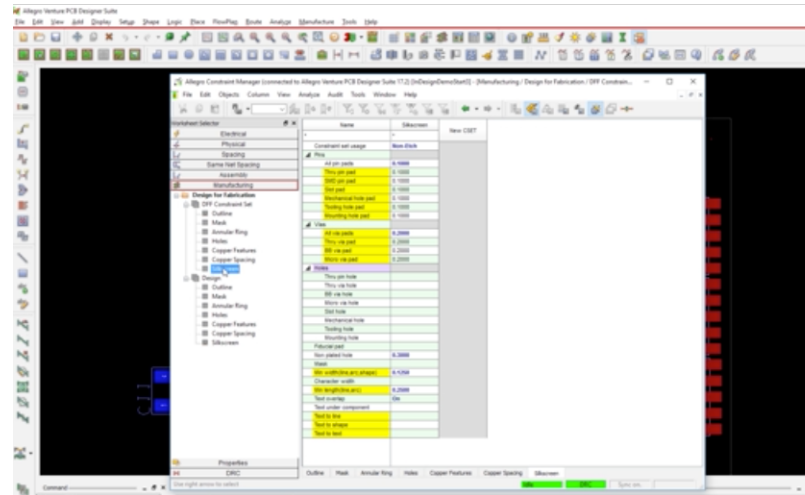
MIPI-M Compliance Kit

- Includes automated jitter tolerance sweeping



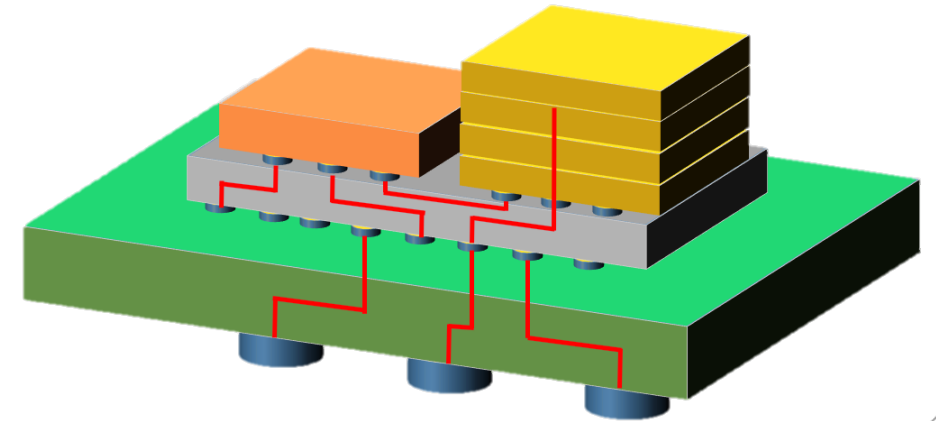
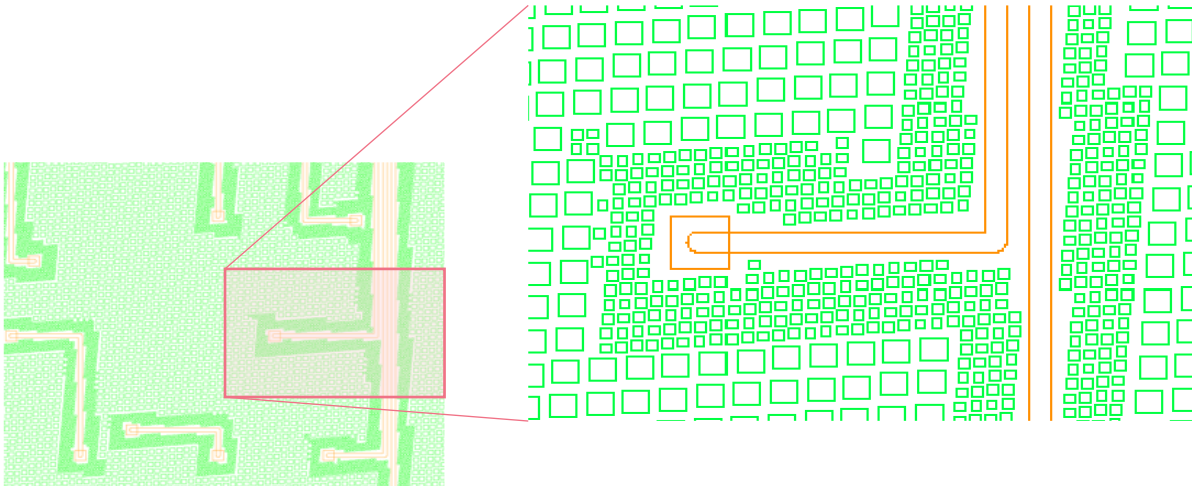
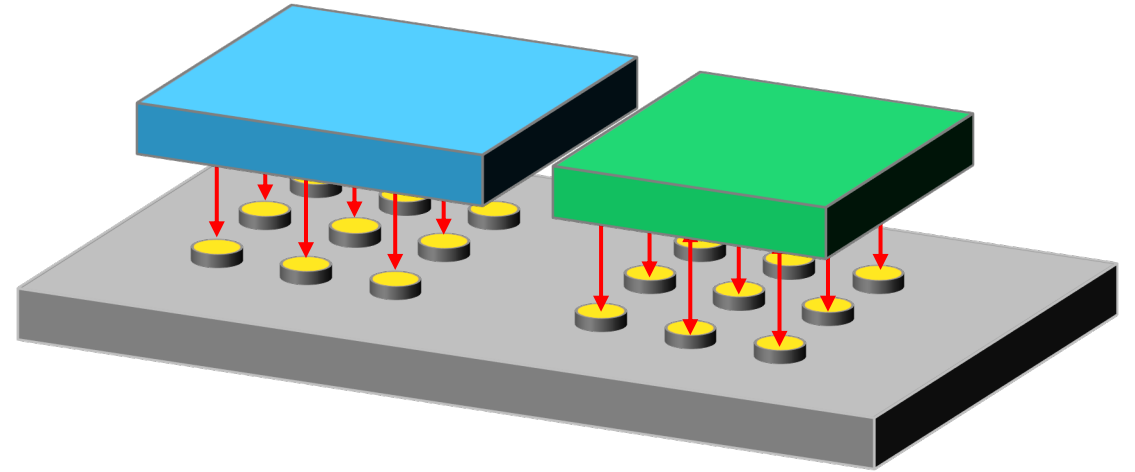
Design for Manufacturability (DFM) – Laminate Substrates

- Rules aligned with substrate providers
 - Conductor rules
 - Soldermask rules
 - Annular ring checks
 - Silkscreen checks
 - Slivers and islands
- Rule aggregation to support multiple sources
- In-Design checking to assure first-pass CAM sign-off
- Automation all DFM documentation



Rule Decks – Semiconductor Foundry Process

- DRC
 - Including 3D stack pin alignment
- LVS
 - Chip(let)-to-Chip(let)
 - System-level
- Metal fill
 - Smart metal balancing



Conclusion



PDKs have been successfully leveraged by the IC design community for decades



Packaging technology is exploding in complexity and designing in the dark is no longer an option



New challenges face both package designers and IC designers and require different solutions



It's time for the package design community to embrace the Assembly Design Kit (ADK)



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