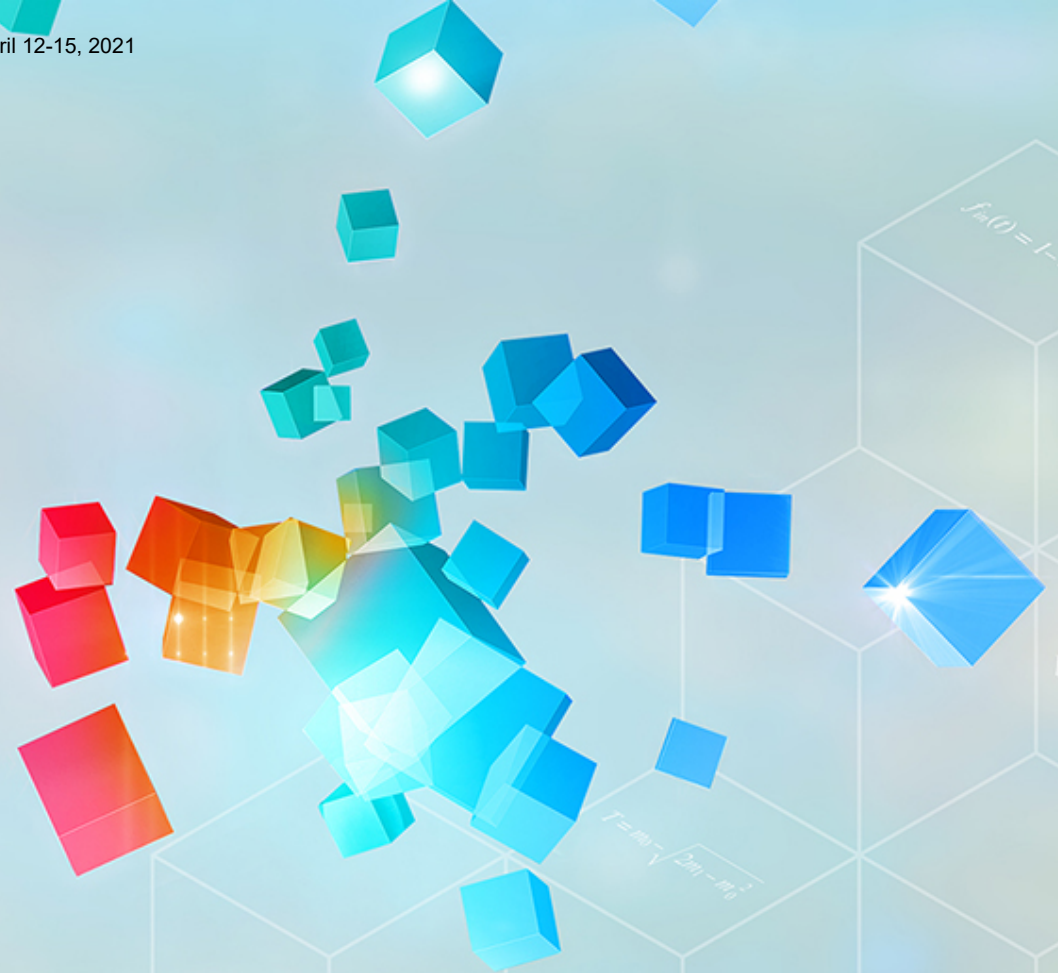


Package Assembly Design Kits

What are they and how they can benefit the packaging community

John Park

Advanced IC Packaging and Cross-Platform Solutions

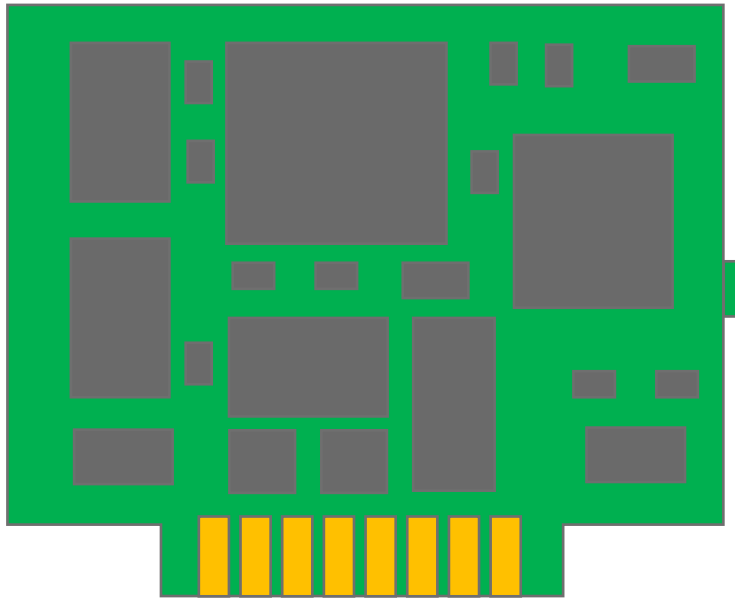
Outline

- Market Trends
- History and purpose of a PDK
- Why it’s time for PDK-like solution for package designers
- Contents of an Assembly Design Kit (ADK)

Chiplet-Based (Heterogeneous Integration) Architectures

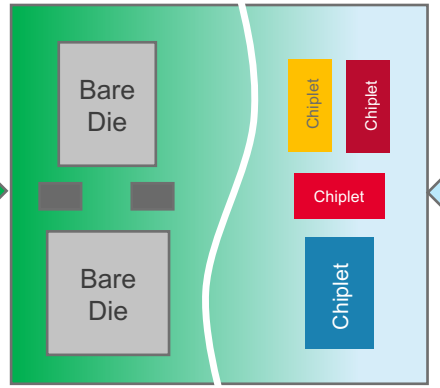
The transition from system on a chip (SoC) to system in a package (SiP)

PCB → Board size/complexity reduction (SWaP) → **Multi-Chip(let) Packaging** ← Disaggregated SoC ← **SoC**



MCM/SiP

Unpackaged die

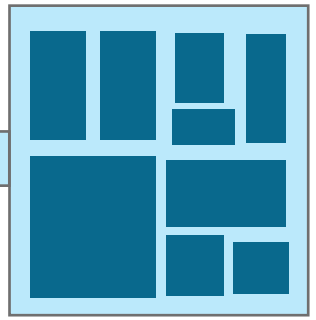


Laminate Substrate

Silicon Substrate

Heterogenous Integration

Chiplets

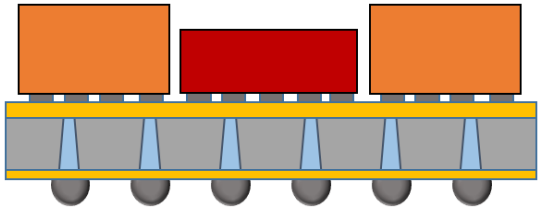


PCB to MCM/SiP Benefits
Smaller footprint
PCB simplification
Higher bandwidth
Lower power

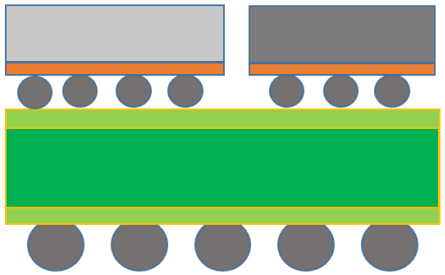
SoC to HI Benefits
Reduced NRE costs
Shorter time to market
Larger than reticle size designs
More flexible architectures

Packaging Technologies Being Targeted for Heterogenous Integration

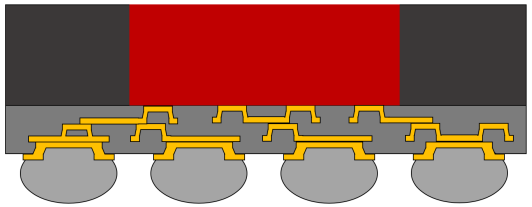
Silicon Interposers (2.5D-IC)



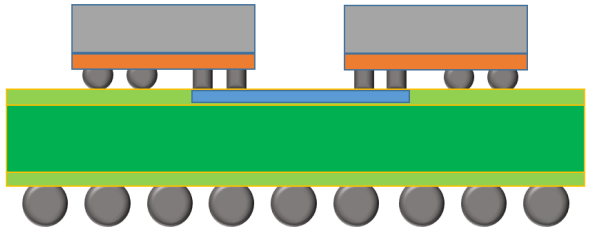
Laminate BGA/LGA



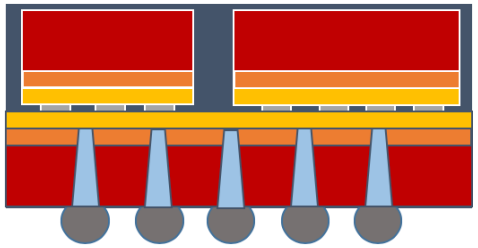
High-Density RDL (FOWLP)



Embedded Bridges



Chip-on-Wafer Stacking (3D-IC)



Outline

- Market Trends
- History and purpose of a PDK
- Why it's time for PDK-like solution for package designers
- Contents of an Assembly Design Kit (ADK)

History and Purpose of a Process Design Kit (PDK)

- The original concept of PDK (Process Delivery Kit) came out of Texas Instruments in January of 1991 with a goal of providing IC designers with everything they need to know, based on the manufacturing process, to design their chip. And to deliver this knowledge through EDA design tools/flows
  - In other words…to connect the manufacturing process with the design process
  - Cadence adopted the concept and renamed the term PDK to Process Design Kit (PDK) in 1993

Paul Koch – Retired Semiconductor Executive

Outline

- Market Trends
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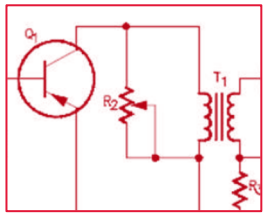
- Why it's time for PDK-like solution for package designers
- Contents of an Assembly Design Kit (ADK)

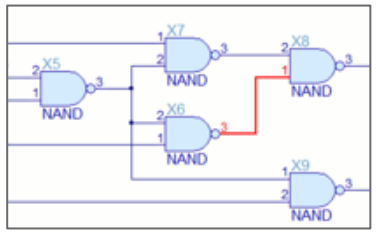
Design and Verification is Only Getting Harder



Transistor-level

1980

Functional

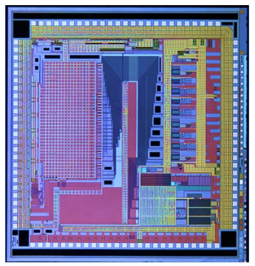


Gate-level

1990

Functional

Timing



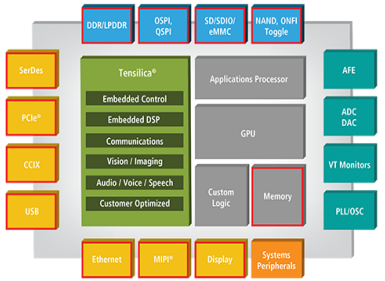
ASIC

2000

Functional

Timing

Power



SoC

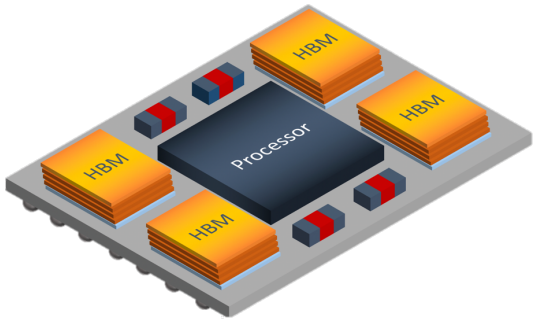
2010

Functional

Timing

Power

Reliability



Heterogeneous Integration

Now

Functional

Timing

Power

Reliability

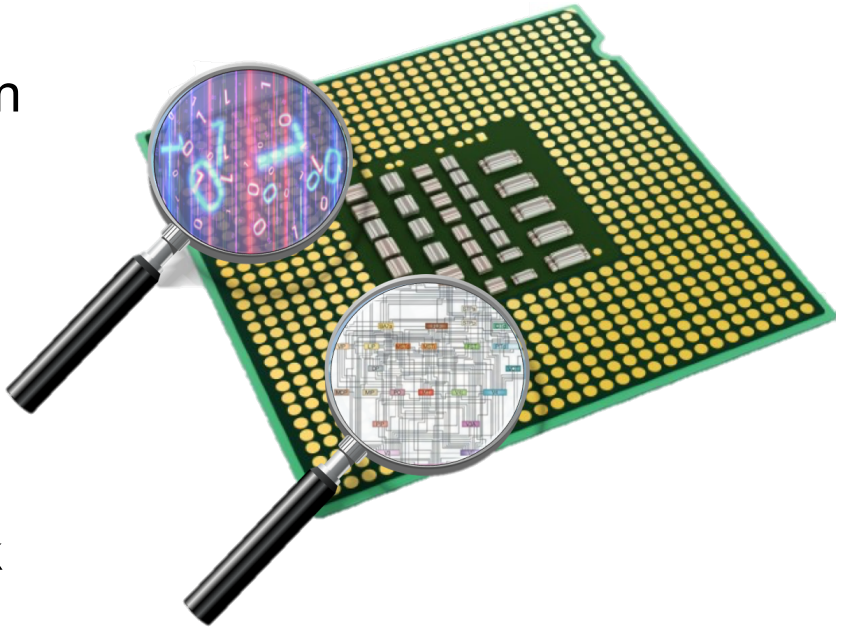
System-Level

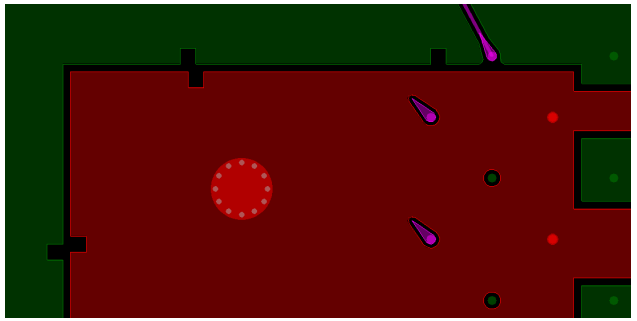
Thermal

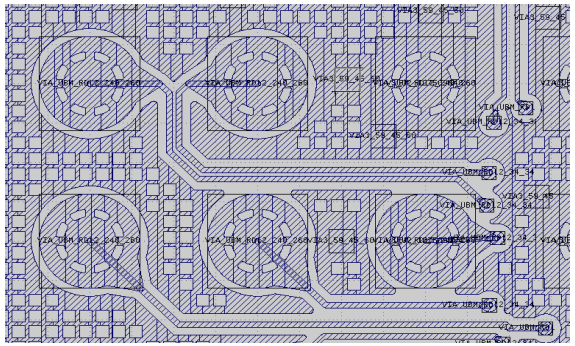
Mechanical

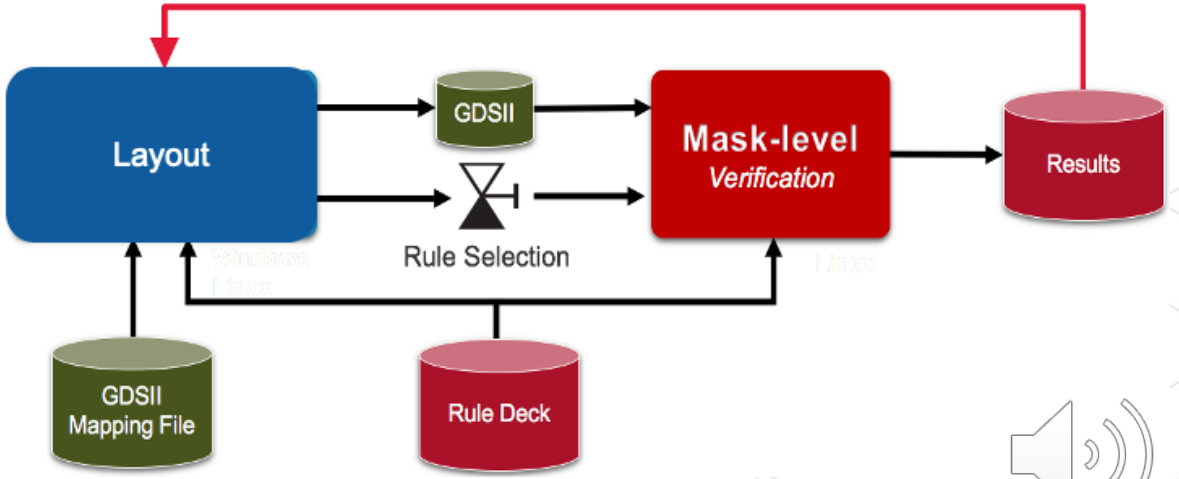
Design Tool/Flow Challenges for the Package Design Team

- Advanced multi-chip(let) silicon-based packages require specialized layout features and formal physical/logical verification capabilities
- Layout features specific to silicon substrate designs
  - Advanced filleting and trace widening
  - Progressive shape and pad degassing algorithms
  - High-capacity design support
- Mask-level accurate output data (GDSII) from substrate layout tool
  - Advanced arc vectorization
- Seamless integration with IC physical verification tool with feedback loop to layout
  1. Mask-level DRC
  2. Connectivity verification (LVS) of multi-chip(let) designs
  3. Region specific advanced metal fill (balancing)



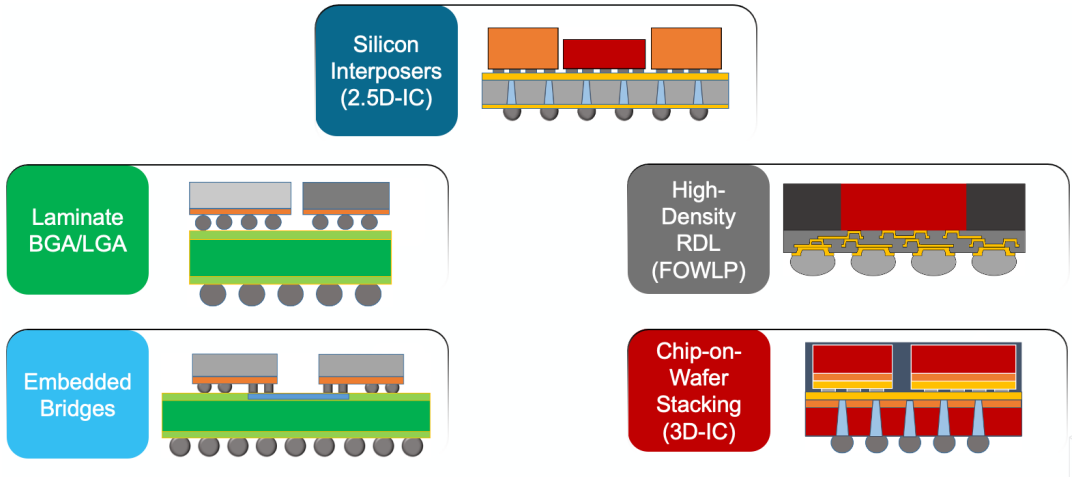






Why We Need ADKs

It’s time for package designers to stop guessing and start knowing



IC designers are new to packaging and package designers are new to IC/silicon substrates

Outline

- Market Trends
- History and purpose of a PDK
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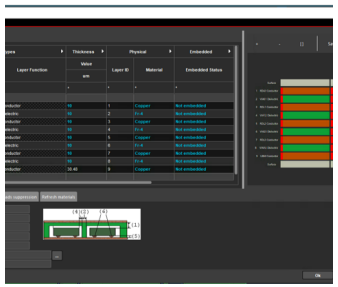
- Contents of an Assembly Design Kit (ADK)

(Package) Assembly Design Kit (ADK)

- Looking Beyond Design-Rule Manuals and Reference Designs…

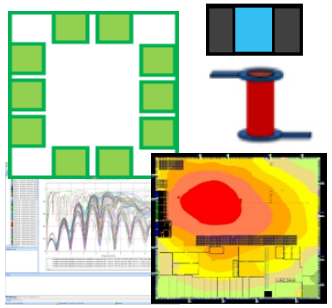
TechFiles



Layer stack-up
- Material
- Properties
- Thickness

Physical/Electrical layout constraints

Design Libraries



Footprints
- Discrete
- BGA/LGA
- 3D Mechanical

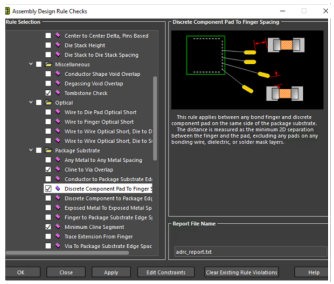
Bond-Wire profiles

IO models

Thermal models

Power models

Assembly Rules

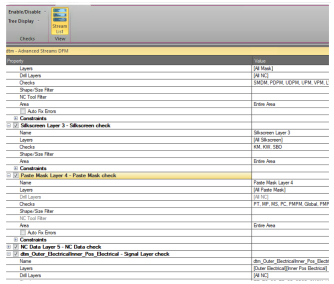


Device placement constraints based on assembly pick & place equipment
- Die to die spacing
- Device to device
- Device to obstacle

Compliance Kits

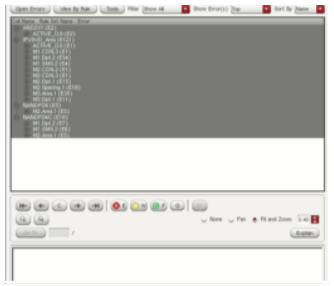
Electrical spec validation of chip(let)-to-chip(let) interfaces
- Jitter tolerance
- Insertion loss
- Return loss
- Eye mask

Manufacturing Rules



Board/substrate manufacturing process
- Substrate checks
- Soldermask checks
- Soldering issues
- Silkscreen checks

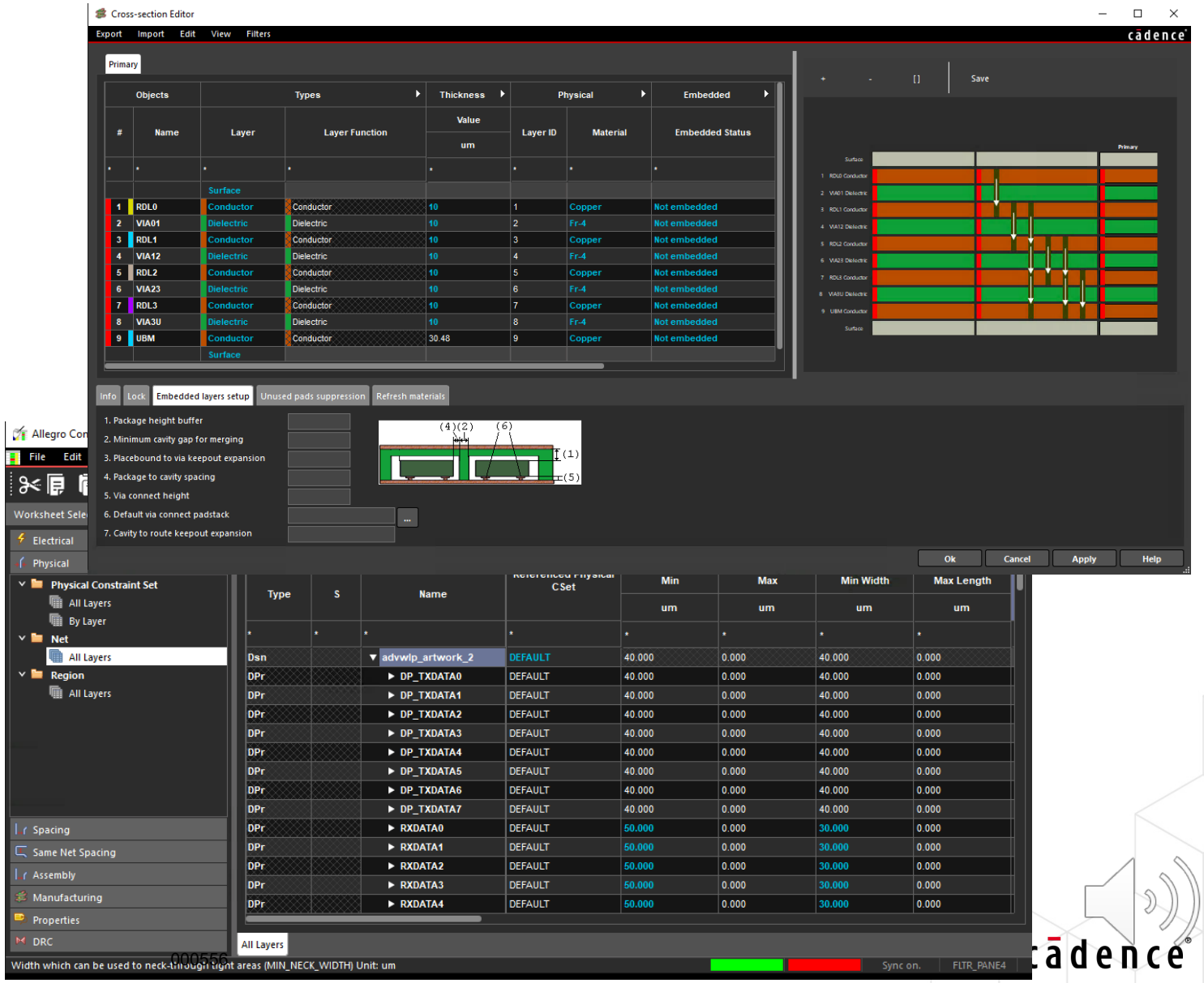
Rule Decks



Foundry/semiconductor manufacturing process
- DRC
- LVS
- Metal fill

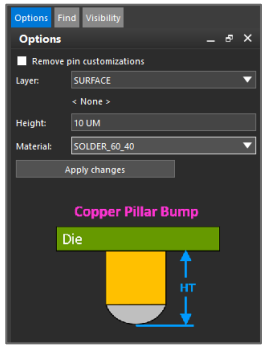
Tech File

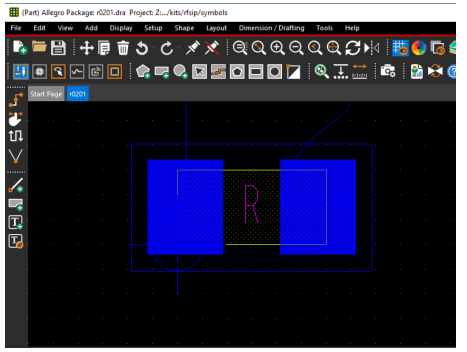
- ASCII file
  - Easy to manage and share
- Read, write and compare
- Re-use
- Contents
  - Substrate stack-up physical and electrical details
  - Physical/Spacing signal constraints
  - Electrical signal constraints
  - Constraint groupings
  - Assembly/placement rules
  - Test rules

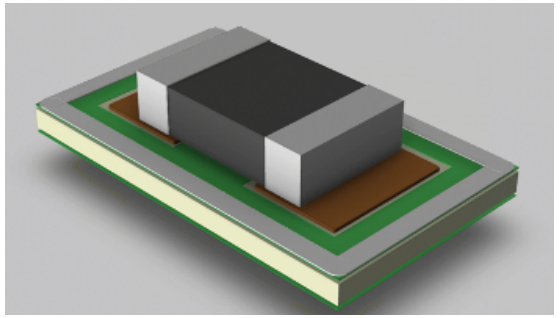


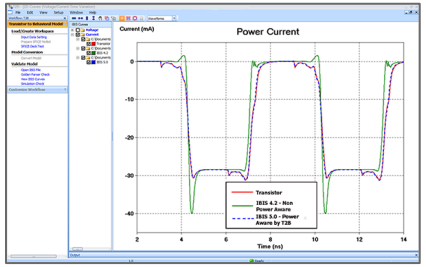
Design Libraries and Models

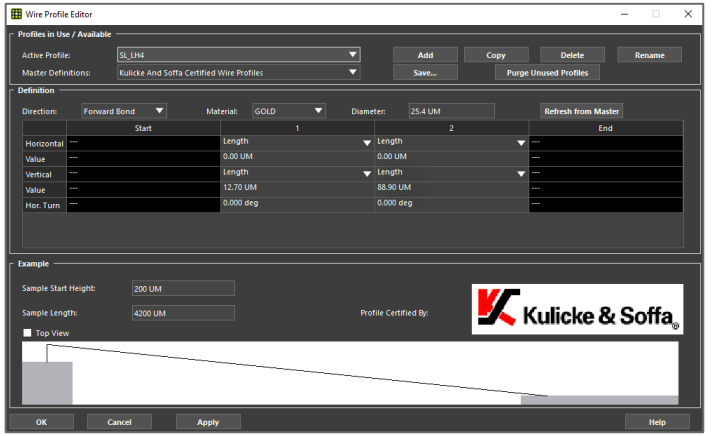
- Footprints
  - JEDEC standard BGA/LGA and SMD
    - Padstacks
  - STEP files (true 3D rendering)
- 3D Bond wire profiles
  - Model based on bonding equipment
  - Required for 3D DRC
- I/O models
  - Behavioral (IBIS)
  - Transistor-level
- Thermal/Power models
  - Chip(let)-level thermal and power models
  - Static and Transient Power information

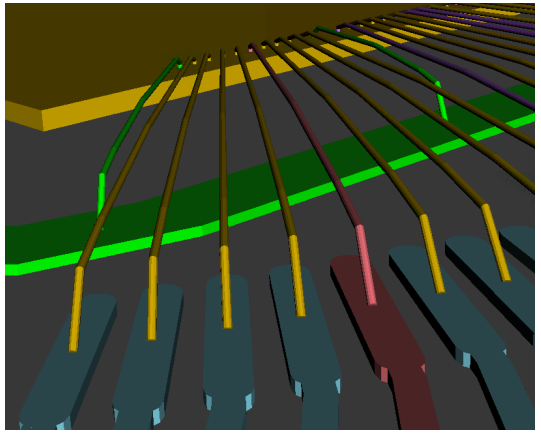


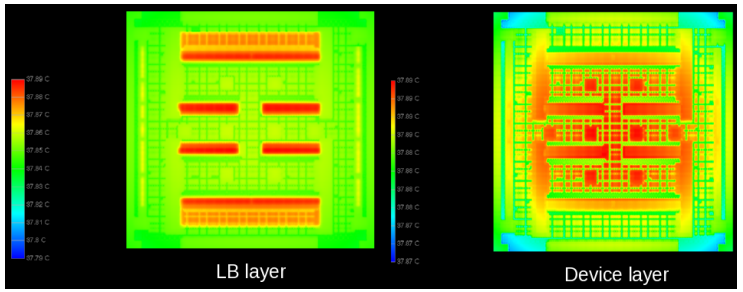


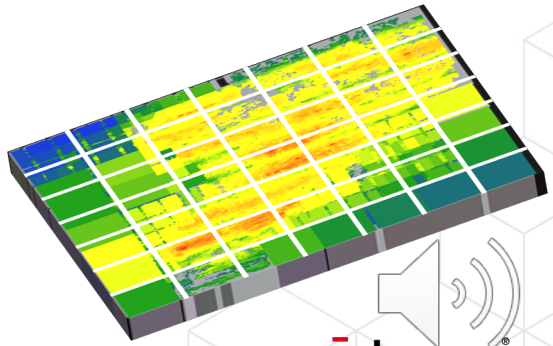








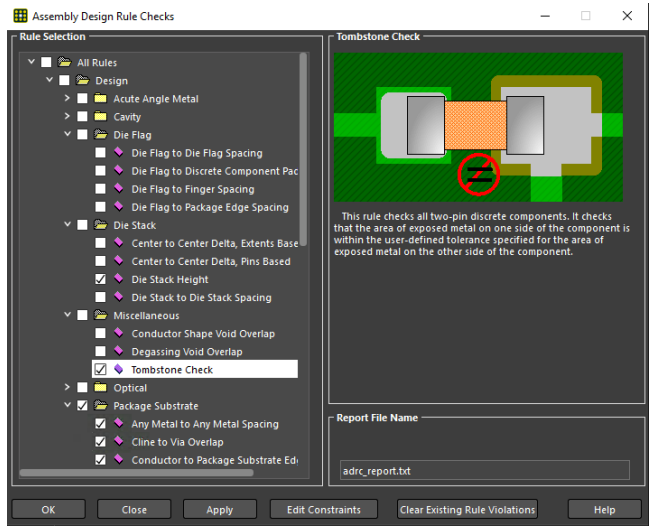


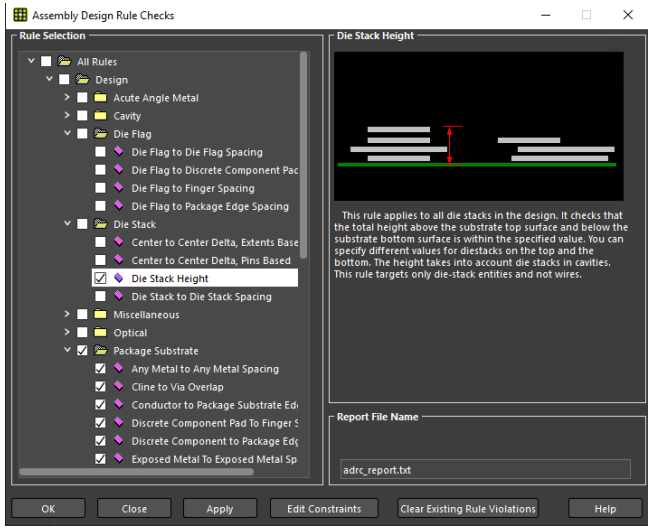


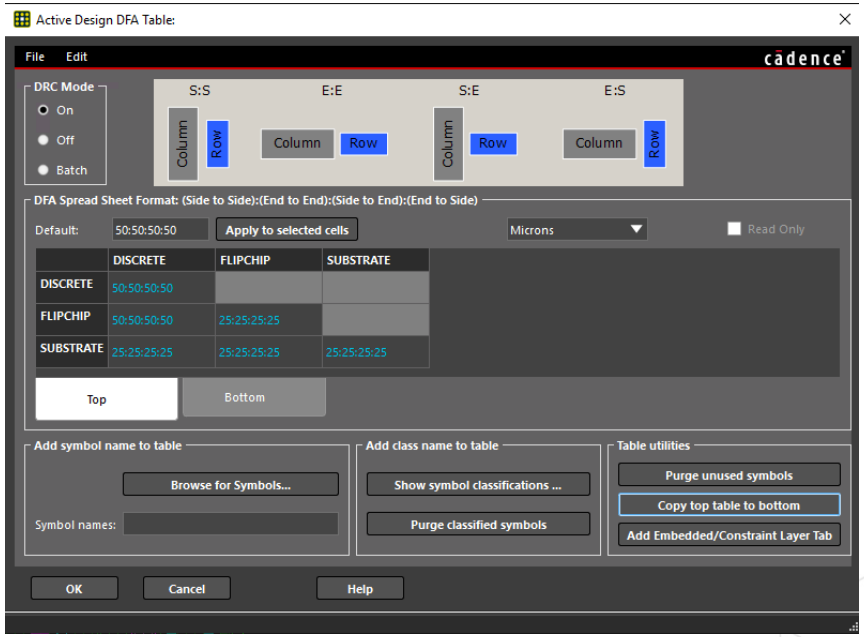
000557

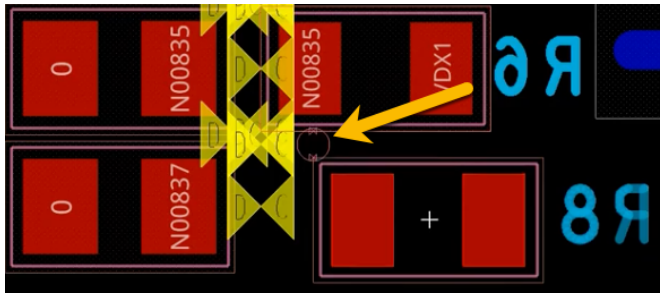
Design for Assembly

- GUI driven assistant to ease setup
- Unique to device DFA outline
- In-design direct feedback during component placement and move
- Table-driven with user defined component categories
- Basic mode (table) and advanced mode (Constraint Manager)
- Rule definition setup can be done in separate tool at the library level



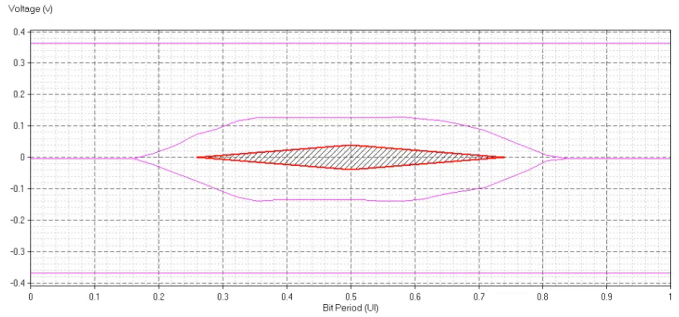


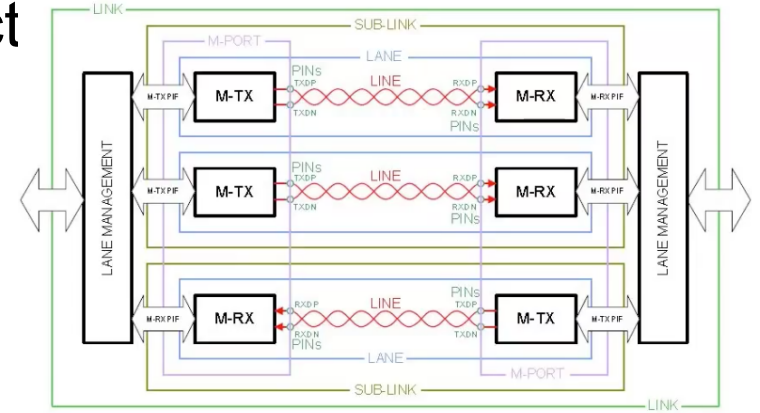


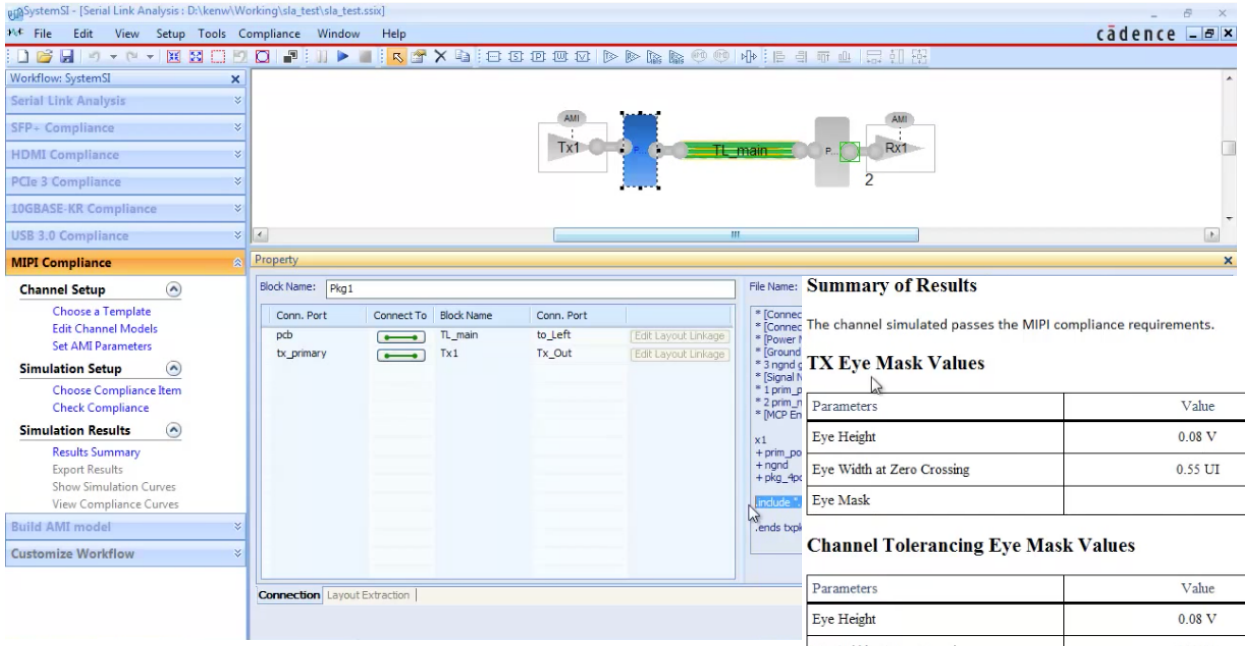


Compliance Kits

- Electrical validation of chip(let)-to-chip(let) interconnect

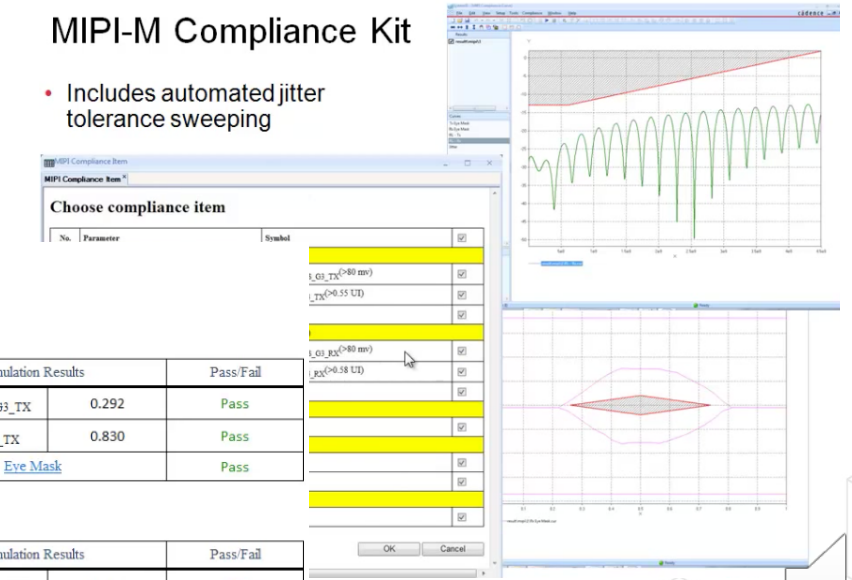






MIPI-M Compliance Kit

- Includes automated jitter tolerance sweeping



Summary of Results

The channel simulated passes the MIPI compliance requirements.

TX Eye Mask Values

Parameters	Value	Simulation Results		Pass/Fail
Eye Height	0.08 V	$V_{DIF\_AC\_HS\_G3\_TX}$	0.292	Pass
Eye Width at Zero Crossing	0.55 UI	$T_{EYE\_HS\_G3\_TX}$	0.830	Pass
Eye Mask		Eye Mask		Pass

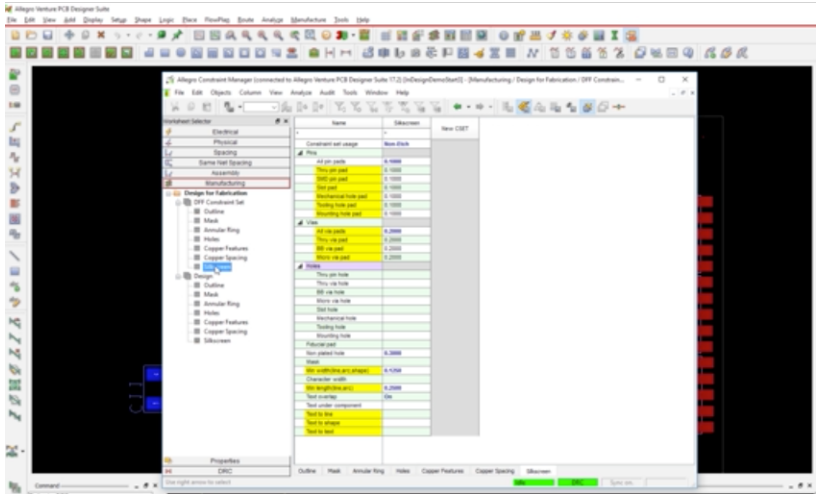
Channel Tolerancing Eye Mask Values

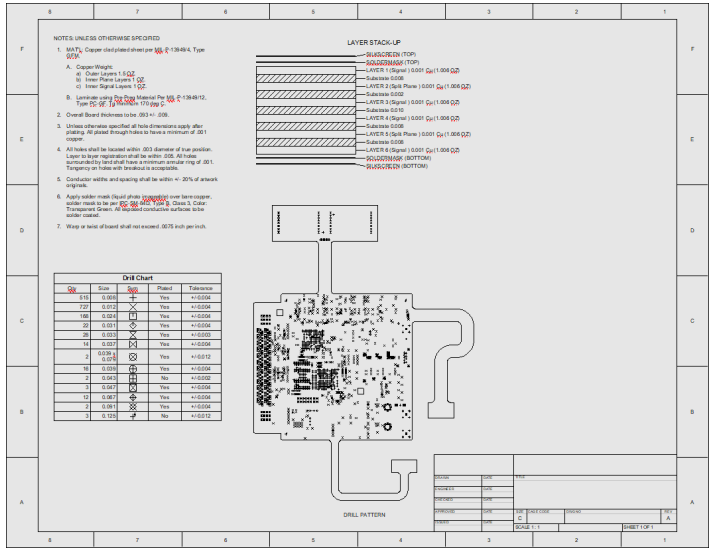
Parameters	Value	Simulation Results		Pass/Fail
Eye Height	0.08 V	$V_{DIF\_AC\_HS\_G3\_RX}$	0.265	Pass
Eye Width at Zero Crossing	0.58 UI	$T_{EYE\_HS\_G3\_RX}$	0.630	Pass
Eye Mask		Eye Mask		Pass

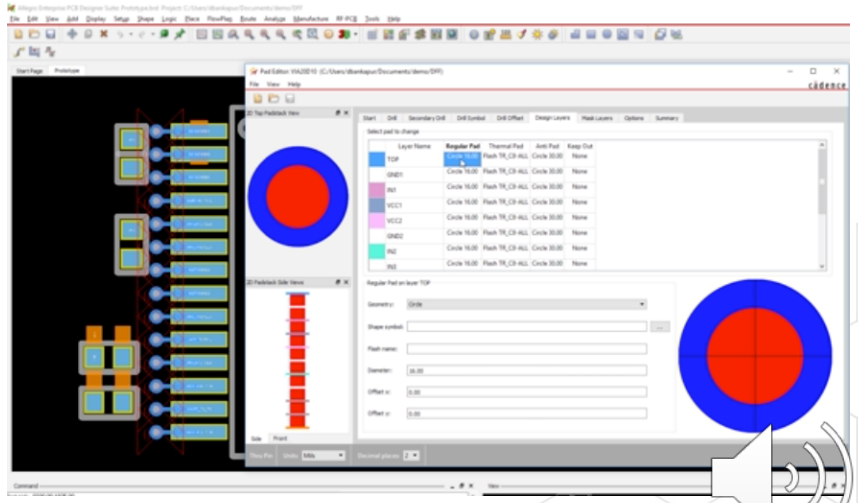
000559

Design for Manufacturability (DFM) – Laminate Substrates

- Rules aligned with substrate providers
  - Conductor rules
  - Soldermask rules
  - Annular ring checks
  - Silkscreen checks
  - Slivers and islands
- Rule aggregation to support multiple sources
- In-Design checking to assure first-pass CAM sign-off
- Automation all DFM documentation

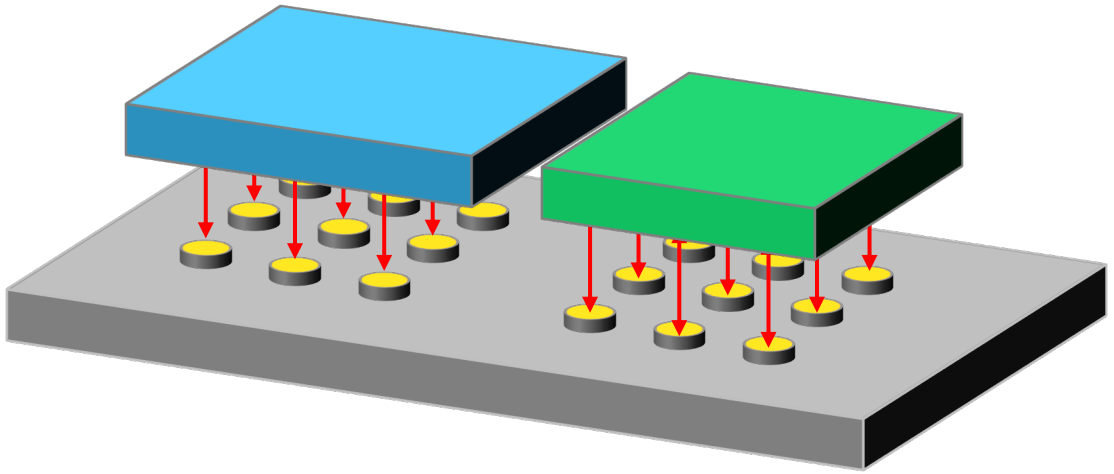


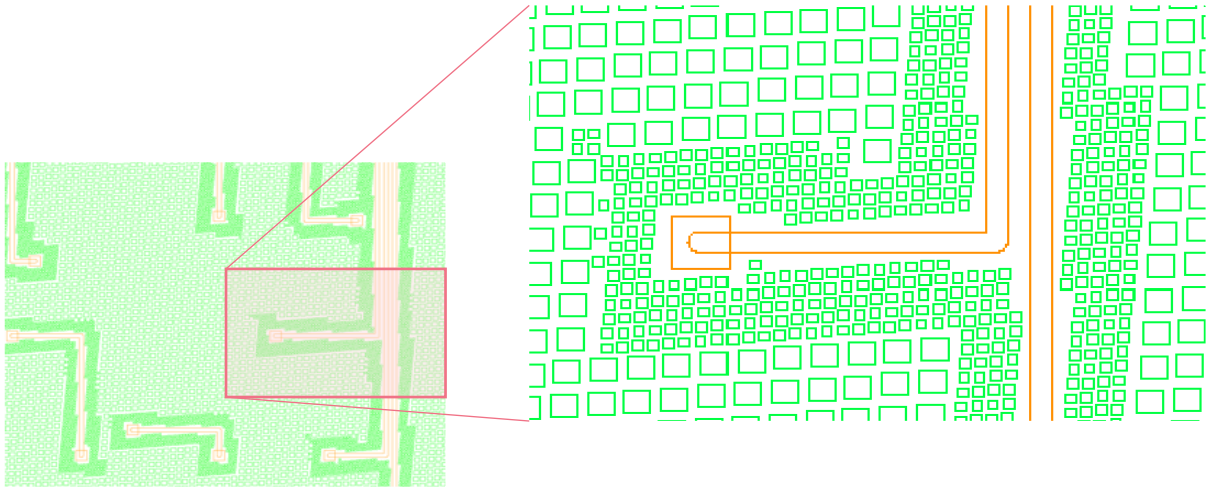


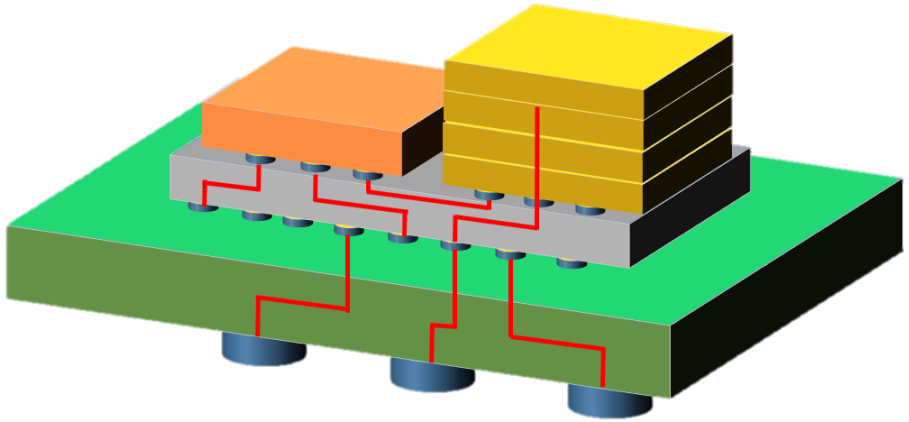


Rule Decks – Semiconductor Foundry Process

- DRC
  - Including 3D stack pin alignment
- LVS
  - Chip(let)-to-Chip(let)
  - System-level
- Metal fill
  - Smart metal balancing







Conclusion